International Journal of Computer Sciences and Engineering Open Access
Research Paper Volume-4, Special Issue-2, April 2016 E-ISSN: 2347-2693

Module Voltage Balancing Algorithm for Phase Shifted SPWM Controlled Cascaded Multilevel Inverter

Suruchi Gupta and S. R. Deore

[1,2]*Department of Electrical Engineering, A. C. Patil College of Engineering, Kharghar, Navi Mumbai*

www.ijcseonline.org

Abstract—Multilevel inverters are considered to be an effective and practical solution for increasing power demands and harmonic reduction. They have been attracting attention because of increased power ratings, better harmonic performance and optimized electromagnetic interferences. Among several topologies proposed in literature, Cascaded H-bridge Multilevel Inverter (CMI) stands out due to its advantage in modularization, extendibility and minimization in number of power semiconductors. But one of the major limitations in case of Cascaded Multilevel Inverter is voltage unbalance across dc capacitors with increase in output voltage levels. The module voltage balancing algorithm such as sorting strategy has been proposed for modular multilevel inverter as well as Level Shifted controlled Cascaded Multilevel Inverter in literature. This paper explores basic operating principle of a seven level Cascaded Multilevel Inverter. Carrier based modulation techniques have been summarized. Also, in this paper the sorting strategy for module voltage balance has been proposed for Phase Shifted (PS) SPWM controlled seven level Cascaded Multilevel Inverter. Total Harmonic Distortion (THD) along with module voltage balancing band has also been analyzed.

Keywords—Multilevel inverters, SPWM, sorting strategy, voltage balance control

I. INTRODUCTION

In recent years, many industrial applications require power equipment's in megawatt range. Large inverters have traditionallysatisfied the ever increasing demand of high power industrial applications which extends from tens to hundreds of megawatts [1]. For a medium voltage grid, it is troublesome to connect only one semiconductor switch [2][3]. Conventional inverters have many limitations at high power and high voltage applications due to switching losses and constraints of device ratings.

Multilevel inverter offers number of advantages as compared to conventional inverters. Multilevel inverter not only achieves high power ratings but also allows the use of renewable energy sources. Multilevel inverter includes an array of power semiconductors and capacitor voltage sources and generates stepped output voltage waveform. The commutation of switches permits the addition of capacitor voltages and allows the output voltage to reach higher values while power semiconductors withstand only reduced voltages. The stepped approximation of sinusoidal waveform using higher level reduces the harmonic distortion of output waveform and stresses across semiconductor devices. The reduced switching frequency of each individual switch of inverter also reduces the switching losses and improves efficiency of inverter [4].

Multilevel inverters are divided broadly into three main topologies: diode clamped (neutral clamped) [5], capacitor clamped (flying capacitor) [6][7] and cascaded multilevel inverter [6][8]. Out of the above topologies, cascaded multilevel topology is most promising because each inverter can be seen as module with similar circuit topology, control structure and modulation. Many modulation strategies have been developed for switching control of cascaded multilevel inverter such as carrier based SPWM [9][10].

II. CASCADED H- BRIDGE MULTILEVEL INVERTER

The building block of CMI is a single phase H-bridge inverter. For a seven level CMI three H-bridge modules are connected in series for a single phase as shown in Figure 1(a). The ac output of each H-bridge is connected in series in order to synthesize a stepped staircase waveform shown in Figure 1(b). By connecting the sufficient number of H-bridge in cascade and using proper modulation scheme, a nearly sinusoidal output voltage waveform can be synthesized. In each H-bridge module, the upper and lower switch in each leg operates in complementary mode. Hence, switching states can be determined by switching states of upper switches. Therefore, according to different switching states of four switches, S1-S4, each module can generate three levels in output voltage +Vdc, 0, -Vdc.

Figure 2 illustrates three phase seven level inverter used for analysis in this paper. There are three H-bridge modules connected in series for each phase. To obtain three phase system the output of three identical structures of single phase CMI are connected in star. For phase A, the output voltage is as follows

$$V_{AN} = V_{a1} + V_{a2} + V_{a3}$$

Where, V_{a1}, V_{a2}, V_{a3} are ac terminal voltages of each H-bridge module respectively. Generally, the number of output phase voltage levels is given by 2N+1, where N is number of H- bridges used per phase.

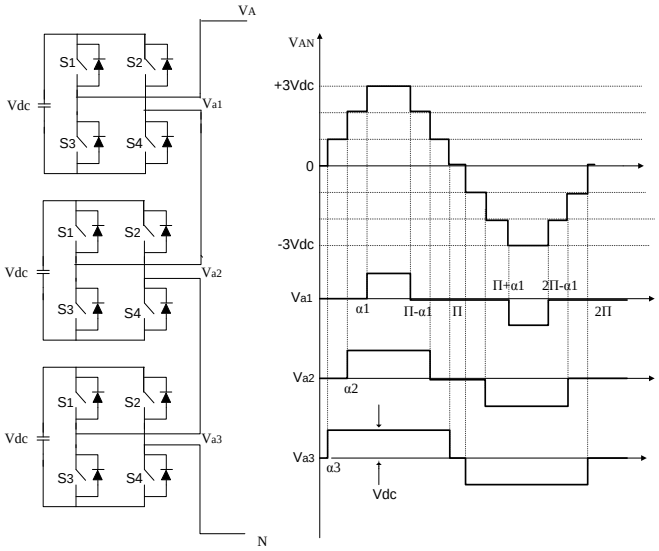

Fig 1(a): Single phase CMI 1(b): Output voltage wave form

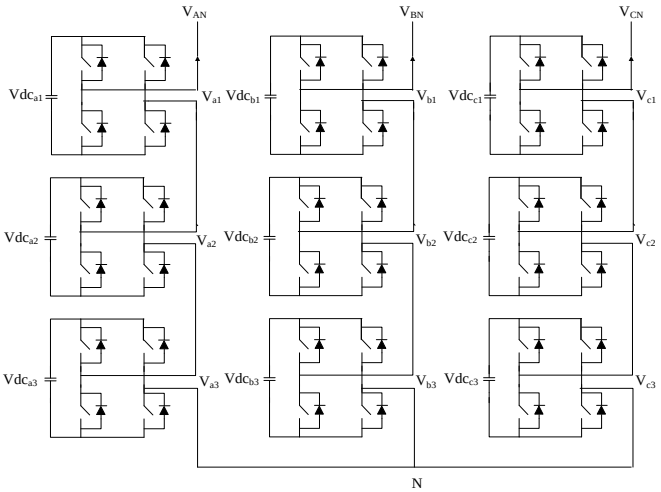

Fig 2: Star configured three phase seven- level CMI

III. MULTICARRIER MODULATION STRATEGIES

Several multicarrier modulation strategies have been proposed in literature to reduce the distortion and minimizing switching losses in multilevel inverter based on classical SPWM with triangular carriers. The basic principle of multilevel carrier Pulse Width Modulation (PWM) technique is to use several triangular carrier signals and one modulating signal. Generally, for an M level inverter, (M-1) triangular carriers are needed. All carrier signals have same frequency and same peak amplitude.

Some multicarrier techniques use carrier disposition and other use phase shifting of carrier signals [11].

A. Phase Shifted SPWM

In this modulation strategy all triangular carriers are phase shifted from each other. The adjacent carriers are displaced by an angle given byΦ= 360 ˚/ (M-1), where M is number of output voltage levels. The carrier waves have same frequency and peak to peak amplitude. Modulating signal is compared with carrier signals to obtain the switching states of each H-bridge. Figure 3 shows the carrier, modulating waveforms and switching function for one phase of a seven level multilevel inverter.When the reference modulating signal is greater than carrier signal, output is 1 during positive half cycle and logic reverses during negative half of modulating signal. The switching function obtained is having half wave unsymmetry.

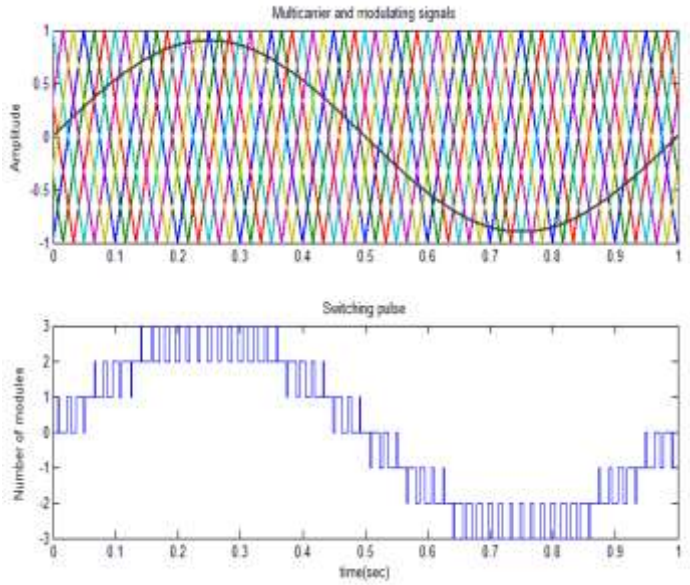

Fig 3: Waveforms for Phase Shifted SPWM

B. Level Shifted SPWM

Level shifted modulation schemediffers from phase shifted SPWM in the disposition of triangular carriers which in this case are vertically shifted.

There are three different PWM strategies with different phase relationships for level shifted multicarrier modulation.

- Phase Disposition (PD)
  In phase disposition, the modulating signal is compared with in phase triangular carrier waveforms which are shifted vertically with respect to zero axis. For M level inverter, (M-1) carrier signals are required. The switching function obtained by comparing modulating signal and carrier signals is having half wave unsymmetry as shown in Figure 4.

- Phase Opposition Disposition (POD)
  Phase opposition disposition, uses (M-1) number of carrier signals, where M is number of output voltage levels. (M-1)/2number of carrier signals are for positive voltage levels and other (M-1)/2 are for negative voltage levels.The positive carrier signals are 180 ˚out of phase with negative carrier signals. Figure 5 represent POD SPWM technique for a seven level multilevel inverter. Modulating signal and all carrier signals are compared to obtain switching function. Switching function obtained in this case has full wave symmetry.

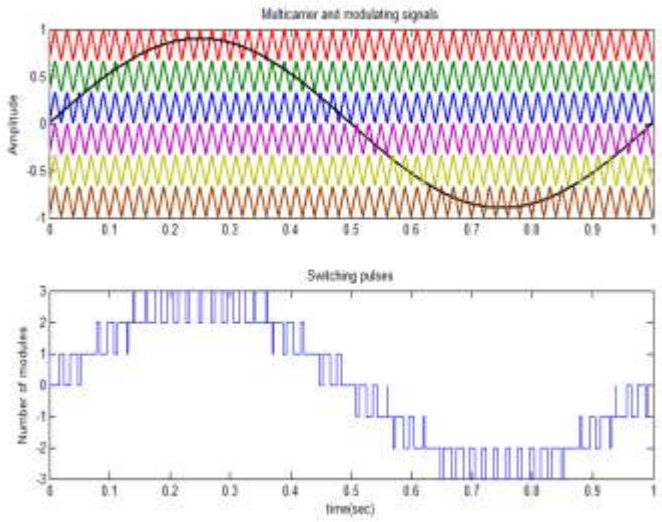

Fig 4: Waveforms for Phase Disposition SPWM

- Alternate Phase Opposition Disposition (APOD)
  In alternate phase opposition disposition, each carrier triangular signal is out of phase with neighboring signal by an angle of 180 ˚. Figure 6 demonstrates APOD SPWM scheme for a seven level multilevel inverter along with switching function obtained by comparison of modulating signal and carrier signals. In this case there exists half wave unsymmetry in switching function.

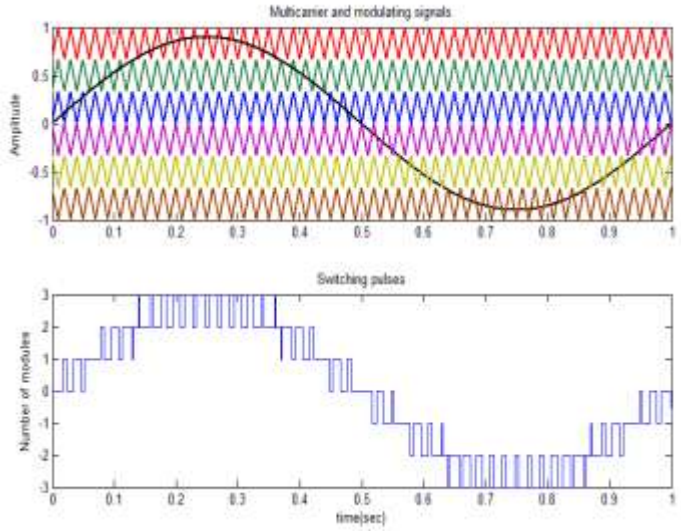

Fig 5: Waveforms for Phase Opposition Disposition SPWM

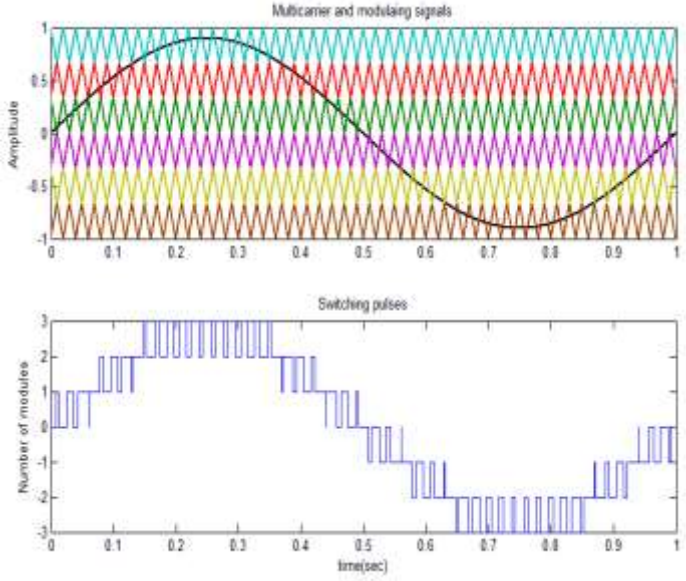

Fig 6: Waveforms for Alternate Phase Opposition Disposition SPWM

IV. OVERALL CONTROLLER OF CASCADED MULTILEVEL INVERTER

The three phase equivalent circuit of CMI connected to ac system is shown in Figure 7

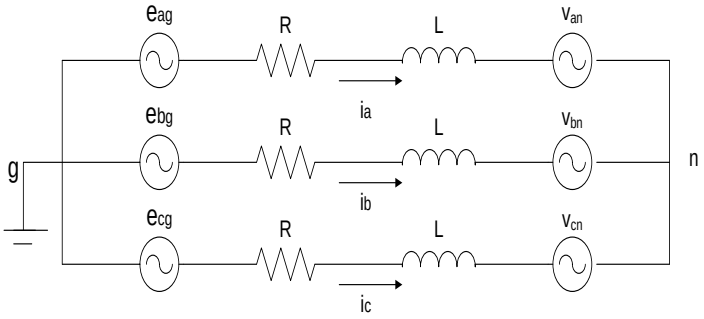

Fig7: Equivalent circuit of CMI

. e_{ag}, e_{bg}, e_{cg} are output phase voltage of inverter and v_{an}, v_{bn} and v_{cn} are source voltage with respect to neutral 'n'. It is assumed that current is flowing from inverter towards the source and is given by

$$I = -\frac{E_c \sin\delta}{X_L} - j\left[\frac{(E_c \cos\delta - V_s)}{X_L}\right]$$

Real and Reactive power as seen from terminals of inverter are given as follows

$$P = \frac{V_s E_c \sin\delta}{X_L}$$

$$Q = \frac{VsE_c \cos\delta - V2_s}{X_L}$$

The control hierarchy of cascaded multilevel converter is shown in Figure 8.

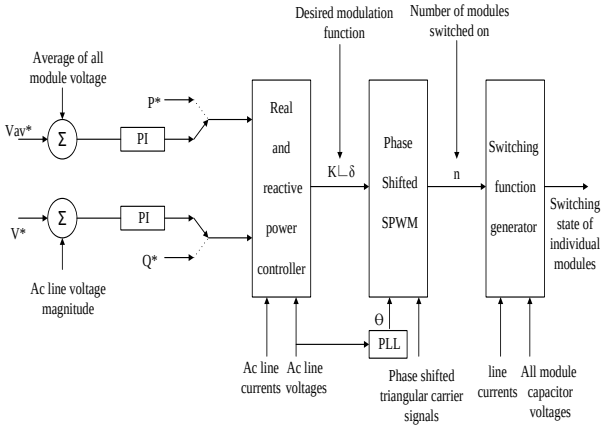

Fig 8:Control hierarchy of CMI [12]

Real and reactive power decoupled components are obtained by converting variables from abc to DQ0 frame of reference. Real and reactive power controller utilize real and reactive power decoupled components to determine modulation index K and angle δ. Depending on the desired amount of reactive power exchange with ac system, inverter output voltage is made to lead or lag by an angle δ with respect to ac system voltage. Phase Shifted SPWM uses PLL output Θ,modulation index K and δ to determine the number of modules to be switched ON. Switching function generator generates the switching function for individual modules according to module voltage balancing algorithm based on sorting strategy discussed later in this paper.

A. Real and Reactive power control

Real and reactive power is determined by fundamental frequency components of line currents. The mathematical model to control real and reactive power is shown in Figure 9. Ac line currents are transformed from abc to DQ0 rotating frame of reference to obtain real and reactive components of current i_Q and i_D respectively. These values are compared with their references i_Q^* and i_D^* respectively and are given to PI controller to obtain inverter output voltages e_Q and e_D given by equations

$$e_D = k_{p2}(i_D^* - i_D) + x_3 + \omega L i_Q$$

$$e_Q = k_{p2}\left(i_Q^* - i_Q\right) + x_2 + v_Q - \omega L i_D$$

Modulation index K and angle δ is obtained from real and reactive power controller as follows

$$. K = \frac{\sqrt{e_D^2 + e_Q^2}}{V_{dc}} \text{and} \delta = \tan^{-1}\left(\frac{e_D}{e_Q}\right)$$

The output of this controller i.e. modulation index K and angle δ isthen combined with PLL output θ to obtain the switching function of each module.

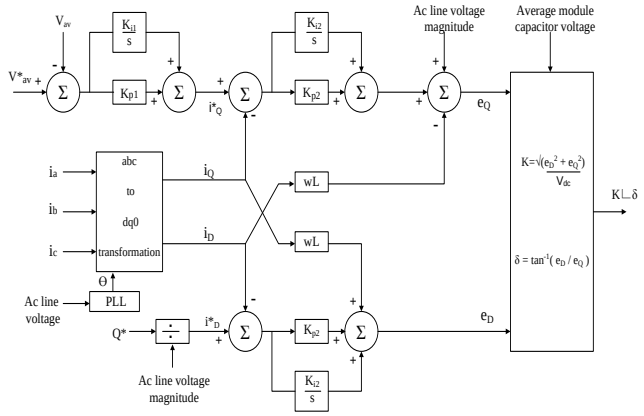

Fig 9: Mathematical model of real and reactive power controller

B. Switching function determination

According to reactive power exchange with supply system, real and reactive power controller determines the modulation index K and angle δ.This can be utilized along with PLL output Θ to obtain desired inverter output voltage waveform as given by set of equations

$$e_{ag} = K\sin(\theta + \delta)$$

$$e_{bg} = K\sin(\theta + \delta - 2\pi/3)$$

$$e_{cg} = K\sin(\theta + \delta + 2\pi/3)$$

The desired output voltage waveform is compared with carrier waveform using Phase Shifted SPWM to determine number of modules to be switched ON. The implementation of above along with sorting strategy determines the switching function of each module.

C. Module voltage balancing algorithm (Sorting strategy)

The main causes of unbalance in module capacitor voltages are due to continuous power loss in switches, capacitors and difference in conduction duration of each H-bridge module due to switching of semiconductors at different instants [13]. All module capacitor voltages of each phase should be maintained at same level to ensure the even sharing of voltage stresses in switches. Balancing can be achieved by module voltage balancing algorithm such as sorting strategy as shown in Figure 10[14].

The block diagram of Phase Shifted SPWM technique along with sorting strategy for determining the switching states of each module is shown in Figure 11. Phase Shifted SPWM technique is used to determine the number of modules 'n' to be turned ON for implementation of desired phase switching function.

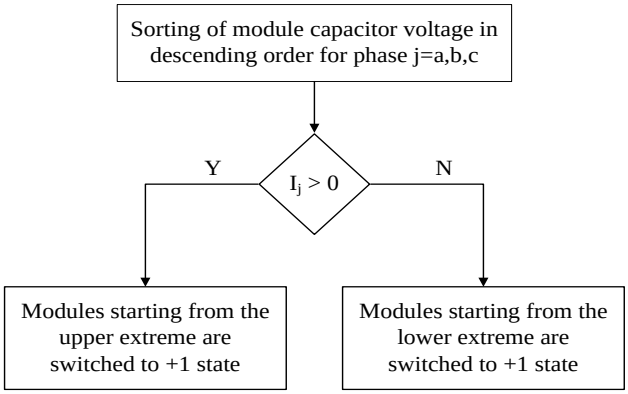

Fig 10: Sorting strategy for H-bridge modules

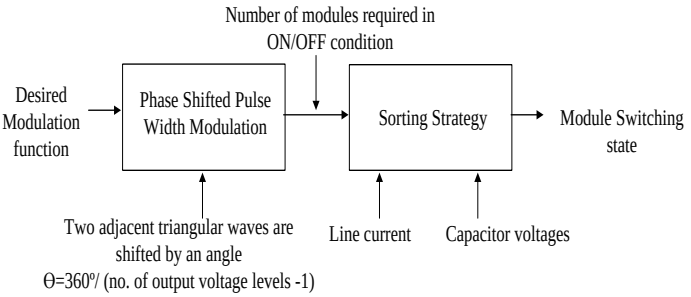

Fig 11: Block diagram of Phase Shifted SPWM along with sorting strategy

The module voltages in a leg are sorted according to their capacitor voltages in descending order. Considering the direction of current as shown in Figure 2, ie from inverter to source, for the positive half cycle of current , the 'n' number of modules from above extreme will be switched to +1 state so that they can discharge. This reduces their voltages. During negative half cycle of current, 'n' number of modules starting from lower extreme are switched to +1 state so that they can charge.

V. CASE STUDY

For simulation study a seven level CMI connected in star having rating of 60 MVA, 11KV is being considered. The leakage reactance X_L is considered to be 0.15 Ω and module susceptance B is of 0.5 mho. The frequency of carrier signals is considered to be 2.5 kHz.

Steady state waveforms are obtained for reactive current reference, $i_D^* = 0.5\,pu$ and module capacitor reference voltage, $v_{av}^* = 0.5pu$

A. Steady state Analysis

Figure 12 shows the steady state waveforms for three phase source voltage, inverter output and line currents using Phase Shifted SPWM. It is observed that for the given sinusoidal ac source voltage the line currents are free from harmonics and inverter output voltage has lower order harmonic contents.

Figure 13 represents steady state waveforms for source voltage, line currents and inverter output voltage for phase 'a'. It also represents the module capacitor voltages for phase 'a'. From waveforms it is observed that inverter output voltage and source voltage are in phase while current leads the voltage waveform. It means that the inverter exchange only leading reactive power with the supply. However, module capacitor voltages vary in broad band but are balanced. This is because of less number of modules and sorting strategy respectively.

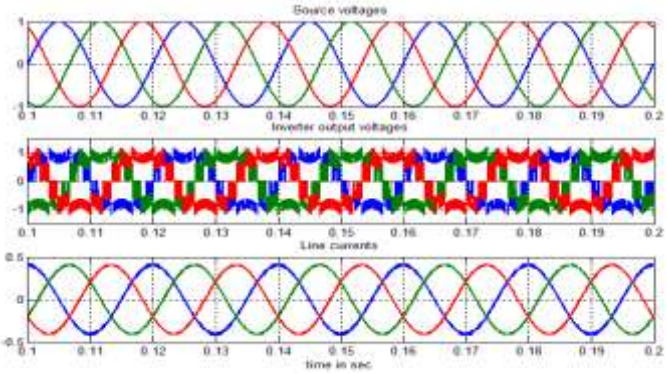

Fig 12: Steady state three phase waveforms for Phase Shifted SPWM

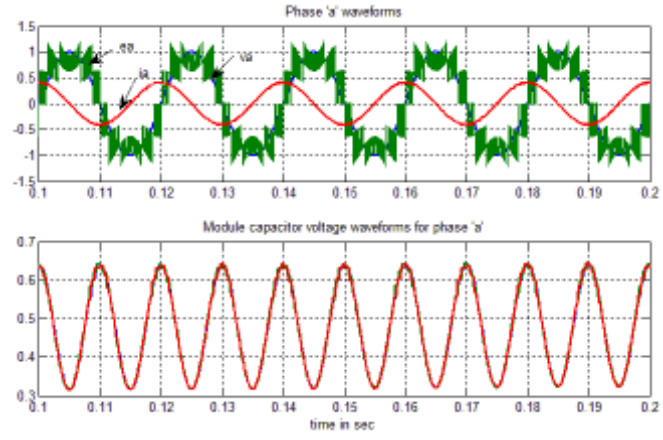

Fig13: Steady state waveforms for phase 'a'

Inverter output voltage and its harmonic spectrum is illustrated in Figure 14. The THD of inverter output voltage is 36.12% and there is a presence of significant third harmonic components.

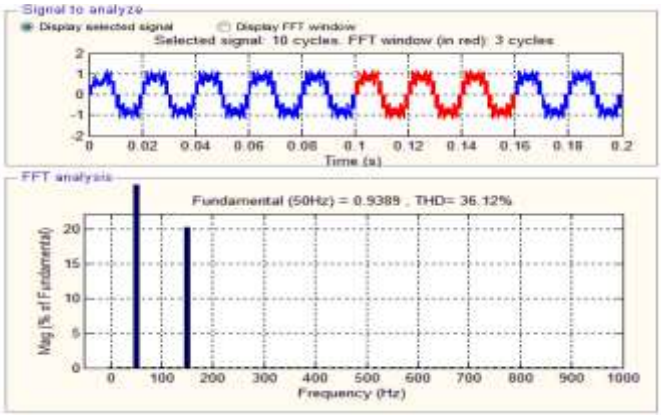

Fig 14: Inverter output voltage and its harmonic Spectrum for Phase Shifted SPWM

B. Voltage Regulation

The controllers of CMI are tested for step change in reactive current reference. Here, initially the set point is i_D^* = 0.5pu and at t = 0.1sec, it changes to 1pu. At t = 0.15sec step change is removed.

Figure15 show the waveform for line currents and reference reactive current for Phase Shifted SWM. It is observed that the response of controller is quiet rapid as expected and settling time is small. However, for i_D^*= 1.0pu the magnitude of line current is more compared to i_D^* = 0.5pu, which is obvious.

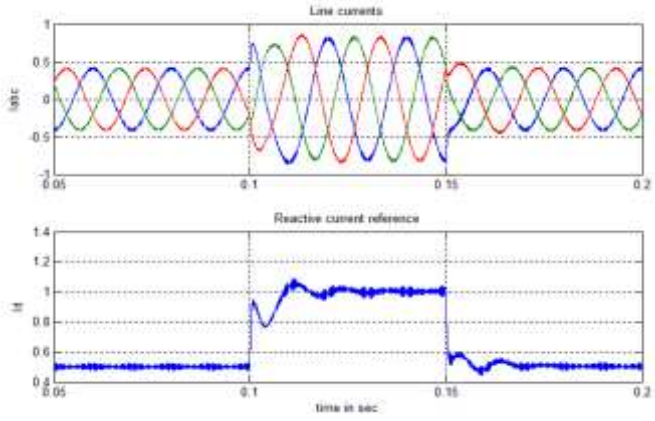

Fig15: Step change in reactive current reference for Phase Shifted SPWM

VI. CONCLUSION

In this paper, a sorting strategy is proposed to balance voltage across capacitors in each H-bridge module of cascaded multilevel inverter. Phase Shifted SPWM is used for implementation of switching function. It can be concluded that module capacitor voltages are balanced but vary in broad range as it is the function of number of modules and switching strategy. Therefore, mathematical analysis of sorting strategy can be possible to reduce the band. The control design of CMI is verified using MATLAB simulations.

REFERENCES

[1] Lin Xu, "Dynamic Modelling, Controls and Electromagnetic Switching of the Modular Cascaded converter (MCC's)", ELEKTRONISKI VESTNIK 80(3): 79-83, **2013**.

[2] X. Zhang, B.Zhang, P. Tang, X. Peng, Y.Luo, ECE Capstone Design Project, Rutgers School of Engineering, Spring**2014**.

[3] S. K. Salankayana, N. Chellammal, R. Gurram, "Diagnosis of Faults due to Misfiring of Switches of a Cascaded Multilevel Inverter using artificial Neural Networks", International Journal of Computer Applications (0975-8887), vol. 41, no.17, March **2012**.

[4] J.Rodriguez, L.G. Franquelo, S Kouro, J.I. Leon, R.Portillo, M. Prats, M. Perz, "Multilevel converters: An enabling t echnology for high power applications" in Proc. of the IEEE, vol. 97, pp. **1786-1817,** Nov. **2009**,

[5] A. Nabae, I. Takahashi, and H. Agaki, "A New Neutral Point Clamped PWM Inverter", IEEE Trans. Ind. Applicat, vol. IA-17, pp. **518-523**, Sept./Oct. **1981.**

[6] J.S. Lai and F.Z. Peng, "Multilevel Converters- A New Breed of Power Converters", IEEE, Trans. Ind. Applicat., vol 32, pp. **509-517**, May/ June **1996**."

[7] T. A. Meynard and H. Fosch, "Multilevel Choppers for High Voltage Applications", Eur. Power Electron. Drives J., vol.2, no.1, pp. **41**, Mar. **1992**.

[8] R. H.B aker and L. H. Bannister, "Electric Power Converter", U.S patent 3867643, Feb. **1975**.

[9] Bin Wu, "High Power Converters and AC Drives", IEEE Press, **2006**.

[10] B. P. McGrath and D .G. Holmes, "Multicarrier PWM Strategies for Multilevel Inverters", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. **858-867**, **2002**.

[11] L.Tolbert and T.G. Habetler, "Novel Multilevel Inverter carrier based SPWM method", IEEE Trans.Ind. Applicat., vol. 35, pp. **1098-1107**, Sept./Oct.. **1999**.

[12] S. R. Deore, P. B. Darji and A. M. Kulkarni, "Switching Function Analysis of Half and Full bridge Modular Multilevel Converter for HVDC Applications", IET Journal on Gen. Trans. and Dist., vol. 7, no.11, pp.**1344-1356**, Nov. **2013**.

[13] L. Tolbert, F.Z. Peng and T. Habelter, "Multilevel Converters for Large Electric Drives", IEEE Trans. Ind. Applicat, vol. 35, pp. **36-44**, Jan./Feb. **1999**.

[14] SuruchiAgarwal and S. R. Deore, "Level shifted SPWM of a seven level cascaded multilevel inverter for STATCOM applications", in IEEE, Int. Conf. on Nascent Tech. in Engg. Field(ICNTE), Navi Mumbai, Jan. **2015.**

Author Profies

Suruchi Gupta received ME degree in electrical (power system) engineering from Mumbai University in 2015. Since 2010, she has been working as Astt. Professor in A.C Patil College of Engineering, Navi Mumbai. Previously worked in Maulana Azad college of Technology, Bhopal

.

S. R. Deore received his Phd in electrical engineering from IIT-Bombay, Mumbai. Presently he is working as Head of Department of electrical department in A. C. Patil College of Engineering, Navi Mumbai.