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Simulation and Designing of Network Signal Booster at 900 MHz

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Abstract— The primary aim of this paper is to present simulation findings and design network signal booster at a frequency of 900 MHz RF. The booster is designed to work on GSM system bandwidth. The gain given by the amplifier circuit was 12dB at the middle frequency with a difference of +-1.3 dB to normalize. The monopole antennas used for signal reception and transmission that have 0.9141-1315i input impedance and -18.18dB return loss. The study includes detailed graphical and tabular view of the results at each design level, simulation.

Keywords— Amplifier, noise figure, Low noise Stability, Impedance matching.

I. INTRODUCTION

A frequency amplifier is formed of three main elements- exterior antenna, amplifier and interior antenna. They form a wireless system to boost cellular reception. A RF-network amplifier is sometimes a repeater system that involves the amplifier adding gain or power to the reception in various directions. There are two antennae one is for transmitting and receiving the signal from the cellular tower also mentioned as outside antenna and thus the work of second antenna is to communicate with the cellular enabled devices [1-3].

The main aim of the RF-network amplifier is taking this telephone cell phone signal around your car, office, workstation or home and amplifying it. After amplification, the signal is rebroadcasted to the area with no reception and weak signal. The result is a boosted telephone reception that reaches the foremost power and brings more signals in your phone even in the foreign places. You will be able enjoy clear calls (the call drop will decrease) and faster internet browsing and rapid data download and upload. This could how all signal boosters work on all technology platform networks including GSM, CDMA, TDMA, HSPA+, and thus the newest LTE.

II. NETWORK AMPLIFIER CIRCUIT DESIGN

Design and simulation of the amplifier circuit is accomplished by using advance simulators. Use the transistor BFG135 and simulate the S parameter file only. The simulation process consists of 4 stages. In each stage a single design is being implemented. Whereas in every next stage, the previously designed amplifier circuit is being customized to achieve the best results. The results, such as gain at each stage are also compared. Coming up with different software models for the transistor, which would also include searching for manufacturer datasheets and s-parameter files with noise data on the internet. For the design of a biasing network include the DC blocking capacitors and RF chokes.

A. Biasing circuit Design

The supply voltage was standardized at 12 VDC. With proper design of biasing resistors, desired operating voltage and current (Vce = 10Vdc and Ic =100mA DC) were achieved. In Figure.2 the values of resistors R1 and R2 are 20 Ω and 12.09K Ω. DC blocking capacitors (C2 and C4) ensure that none of the DC current flows away from the transistor in the RF path. C7 is a filtering capacitor that grounds any high frequency ripple from the DC power supply (VCC). The values of C2, C4 and C7 are 10uF, 10uF and 18pF respectively. The RF chokes (L1 and L2) ensure that no RF signal flows into the DC biasing circuit. RF chokes should be designed to keep out our center frequency from the DC biasing network. The values of RF Chokes are calculated from the formula: $XL = 2\pi f(L)$ (1)

According to this formula the value of RF Chokes is 45nH; however, during simulation it was observed that it is possible to tune all the reactive components simultaneously for maximum gain.

B. Stability sub circuit Design

The amplifier circuit should be unconditionally stable from 0Hz to f_{max}. . Here f_{max}. is equal to the maximum frequency of oscillation of our transistor, BFG135. The maximum limit of frequency range up to 3GHz (It is safe to assume that if the amplifier circuit is stable up to 3GHz, at higher frequencies. The losses of the components and transmission line segments are so high that the reduced gain will negate any possibility of instability). There are two types of tests to check the stability of amplifier circuit (K-Δ test and μ test). The test used for the measurement of the stability of amplifier circuit is derived stability factor μ. [4]

The simulation results of amplifier circuit show that the amplifier circuit is unstable below 500MHz frequency (μ<1). One idea is to add a shunt resistance in the output circuit and tune all component values again to achieve best gain, noise figure and unconditional stability.

C. Matching Circuit Design

The amplifier should be impedance matched perfectly to 50 ohms at input and output around 900MHz. However, there are usually two methods by which impedance matching can be done, each with its unique advantage. It is possible to either match for maximum gain, using technique of simultaneous conjugate matching. [5]

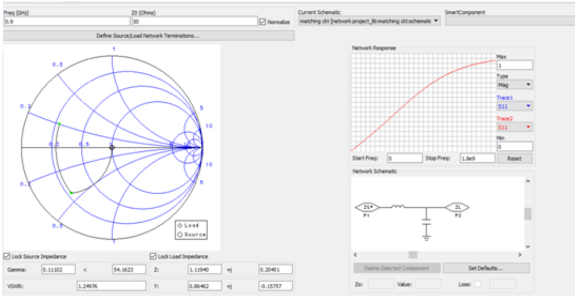

Figure 1. Matching Circuit design using Smith Chart

However, after continuous tuning of all parameters to achieve best noise figure and gain, the matching components no longer retained their designed values. Once the passive matching components are derived, they are inserted in the correct order starting from source and load impedances. Then the schematic components are again tuned for best gain, noise figure and stability. The values of inductor and capacitor for the matching circuit are calculated from smith chart and the values for inductor and capacitor are 5.6nH and 6.24pF respectively. The schematic obtained after inserting the matching components is shown in Figure.2 [6]

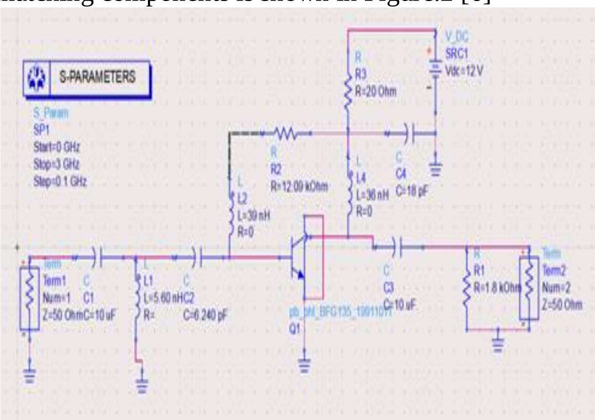

Figure 2. Network Signal Booster

III. SIMULATION RESULT

Given below is the simulation result for the amplifier circuit designed.

Gain: Simulation result show that small signal gain of the amplifier circuit is 12.043dB at 900MHz.

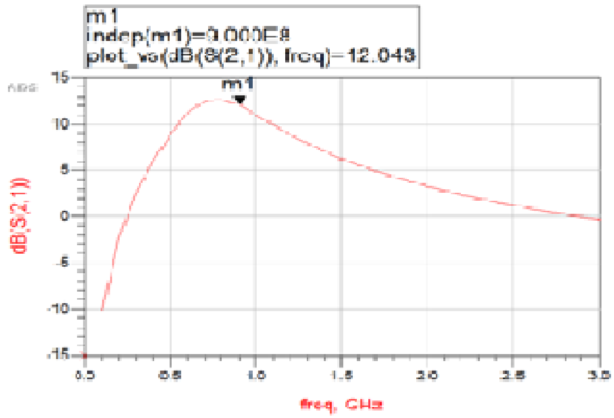

Figure 3. Gain of Circuit

Noise: The most commonly accepted definition of the NF (noise figure) is:

$$NF = SNR_{IN}/SNR_{OUT} \quad (2)$$

where SNR_{IN} and SNR_{OUT} are the signal-to-noise ratios measured at the input and output respectively. NF is a measure of how much the SNR is degraded when a signal passes through a system.

The NF of the LNA is showed in Figure 4. At 900MHz the LNA presents NF=3.93dB. [7].

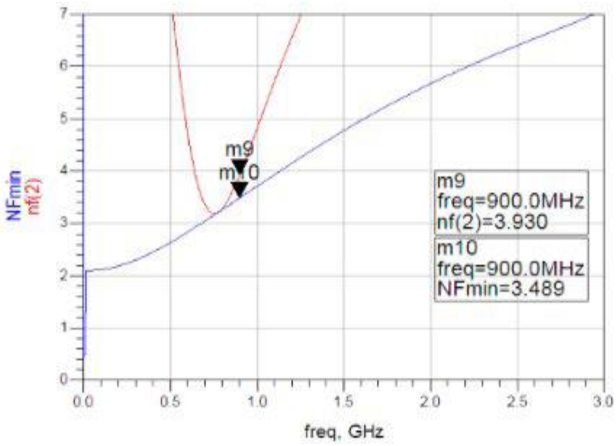

Figure 4. Noise Figure of circuit

Reflection coefficients: Results shows that input and output are not 50Ω matched so we need to apply appropriate LC circuit for impedance matching. After applying matching network the value of input and output reflection coefficients on linear scale (Figure.5 & 6). Smith chart results show that input is exactly matched to 50Ω and output is also matched but not exactly matched to 50Ω. Linear scale results show that value of reflection coefficient at 900MHz is -38.56dB. [8-9]

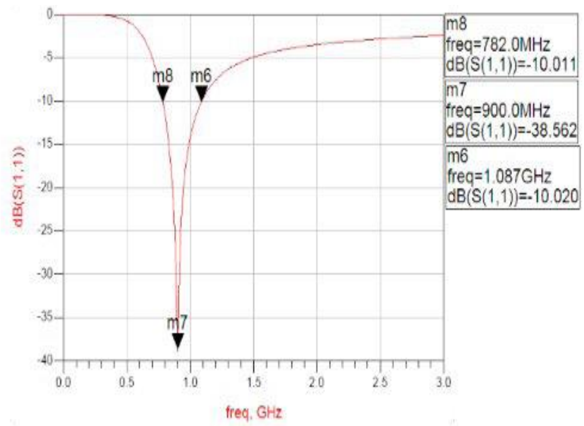

Figure 5. Input reflection coefficient

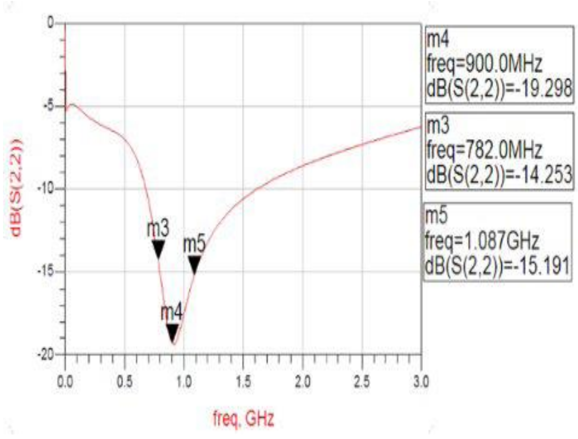

Figure 6. Output reflection coefficient

IV. ANTENNA

The monopole antenna is a resonant antenna; the rod functions as an open resonator for radio waves, oscillating with standing waves of voltage and current along its length. Therefore the length of the antenna is determined by the wavelength of the radio waves it is used with. The most common form is the quarter –wave monopole antenna in which the antenna is approximately one quarter of the wavelength of the radio wave as shown in figure.7.[10-11]

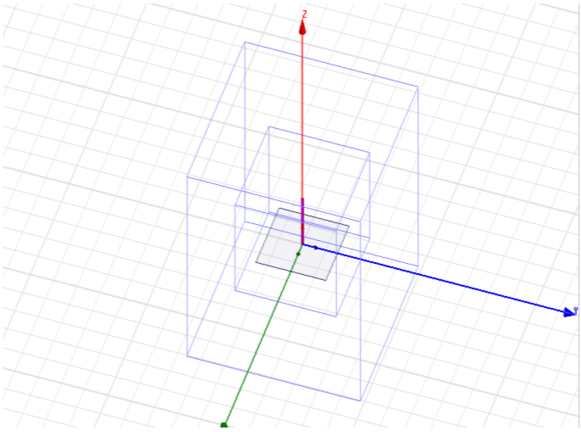

Figure. 7. Simulated monopole antenna

V. SIMULATION RESULTS OF ANTENNA

Given below are the simulation results for the antenna designed.

Gain: Simulation results shows that gain of the monopole antenna is 5.2dB at 900 MHz with S21 parameter**.**

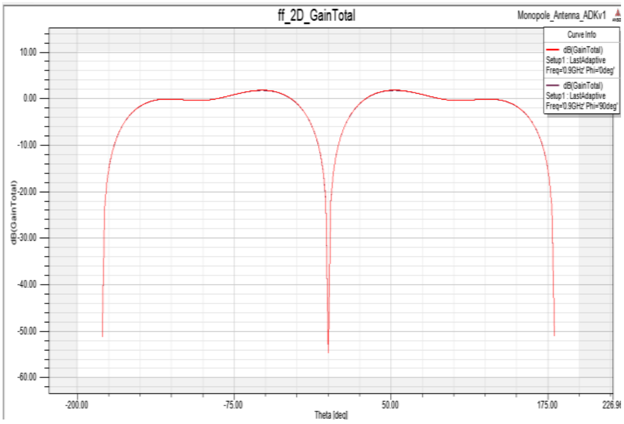

Figure 8. 2D gain of antenna

Return loss: The return loss of monopole antenna at 900 MHz frequency is -18.18dB the simulated result is shown below in figure 9.

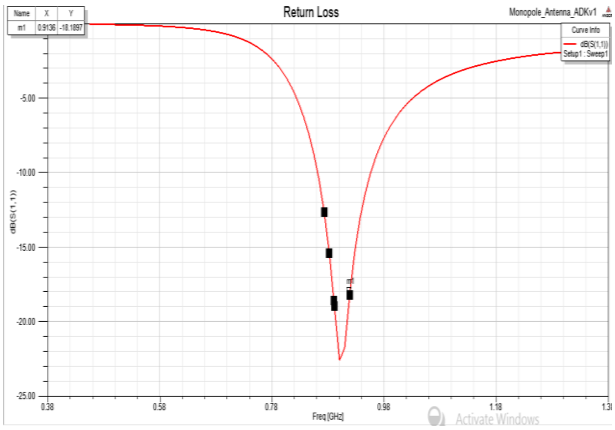

Figure 9. Return loss of monopole antenna

Input impedance: The normalized input impedance for that transmission line is read from the Smith Chart to be read from the Smith Chart is 0.9141+0.1315i as shown in figure 10.

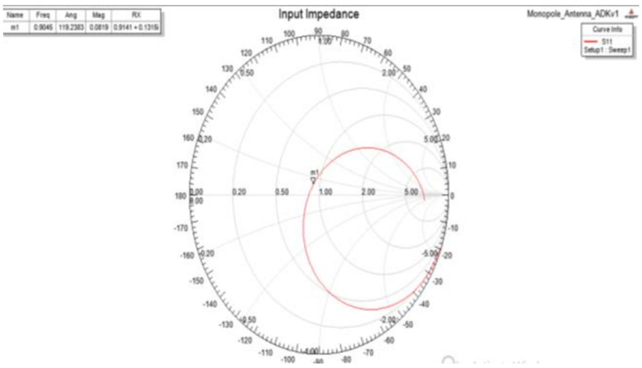

Figure 10. Input impedance of antenna

VI. CONCLUSION

In conclusion, an RF amplifier circuit and monopole antenna at 900MHz was designed, simulated, and built. The amplifier circuit and antenna specifications are shown in **Table 1 and 2**. The amplifier has a relatively high gain – to achieve this gain and yet keep the amplifier inherently stable over all frequencies is a difficult requirement. The only suitable method for satisfying both these divergent specifications simultaneously was to use a series resistor in the input of the transistor. This series resistance has its own undesirable side-effects, notably increase in the noise figure of the entire amplifier circuit.

However, this research work has taught a great deal about RF circuit and monopole antenna design and implementation. It taught about the dynamics and relations between the different constituent blocks of an RF system and how each component affects (or does not affect!) the overall output. Another learning is that simulation software are mainly for understanding these inter-block dynamics and not for calculating the final values of the components unless Trial and error in the final implementation stage is just as important for obtaining optimum results; where the simulation software predicts in which direction the next trial component should be chosen.

Table 1. Specifications of amplifier

SR NO.	Specification	Final value
1	Center frequency	900Mhz
2	Bandwidth	305Mhz
3	Gain	12.04dB
4	Noise figure	3.9dB
5	Impedance matching	50
6	Operating voltage	12v
7	Current consumption	100mA

Table 2. Specifications of antenna

SR NO.	Specification	Final value
1	Length of antenna	7.5cm
2	Operating frequency	900Mhz
3	Input impedance	0.9131+0.1315i
4	Return loss	-18.18dB
5	Ground plane width	15cm

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Human language with all its development is still imperfect. I became aware of it all the more on trying to express the depth of gratitude I feel. Nevertheless, failure in my abilities to express what I feel cannot refrain me from a soul felt esteemed for microwave lab of DIT University in completing this project on **”Simulation and designing of Network Signal Booster at 900Mhz”.** My indebtedness to them is incalculable which cannot be expressed in words. Last of all I would like to dedicate this work to my parents whose toilsome efforts, affection, constant inspiration helped me to complete this work.

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