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Design of a Novel Ring VCO with low Phase Noise and High frequency range

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***Abstract*—** In this paper a ring VCO with high frequency range and low phase noise in 0.18 um CMOS technology is presented. In the proposed VCO, two techniques including current control and forward bias of body is implemented to increase the range of frequency. It is shown that forward bias of the body of control transistor cause to increase the frequency range noticeably. Moreover, by adding an inductor in the body of control transistor, the phase noise is decreased as well. The phase noise in 1 MHz offset frequency is -90 dBc/Hz and the frequency range is 2-14 GHz.

***Keywords*—** VCO, Ring, Phase noise, Frequency range

1. Introduction

PLL (Phase Locked Loop) has wide range of applications in communication and wireless systems[1]. It can be used for time base generation and synchronization circuits in digital ICs as well as phase detection and demodulation in analog circuits[1]. Figure 1 shows the block diagram of a PLL circuit. The heart of a PLL is voltage controlled oscillator (VCO) that can be implemented using LC or ring oscillators [2, 3].

LC oscillators use small value of capacitor and inductor [4] which usually have low quality factor. The low quality factor causes large phase noise and narrow tuning range. Therefore, LC oscillators are mostly used in high phase noise and narrow tuning range applications[5]. Furthermore, large spiral inductors consume a large chip area that is not desirable for integration.

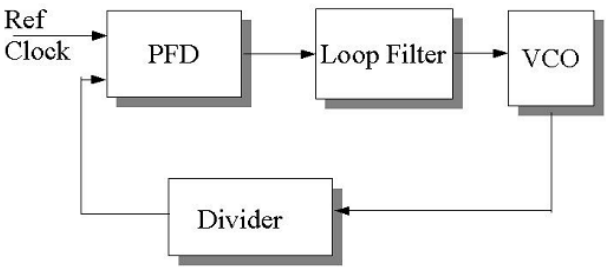

Figure1. A typical PLL circuit block diagram

Ring voltage controlled oscillators (RVCO) have lower phase noise than LC oscillators and because of the wide tuning range, they are used in PLL circuits. In addition, because of smaller chip area comparing to LC oscillators, it is easier to integrate them in a CMOS technology. A ring oscillator consists of multiple gain stages (delay cells) in a loop [4,6] as shown in Figure 2. Different delay cells have been compared in terms of different parameters such as tuning range, power dissipation and phase noise. The delay cells can be differential or single-ended units. Differential configuration is more common because of common mode noise rejection capability, but uses larger chip area and consume more power[3]. The challenges in the RVCO design are to achieve linearity of frequency modulation, low voltage and power Consumption, low phase noise and wide frequency range [7].

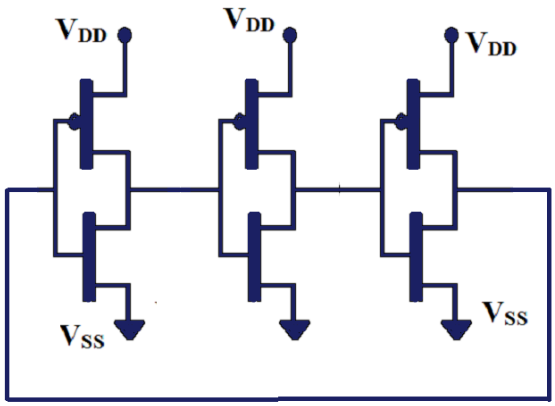

Figure 2 A ring oscillator consists of multiple delay cells

A single-ended oscillator should contain odd number of delay/gain stages with π/n delay value for each stage in a feedback loop [8]. Most reported designs use single ended or differential configuration using current controlled (CC) or voltage controlled (VC) technique as shown in figure 3[4,9].

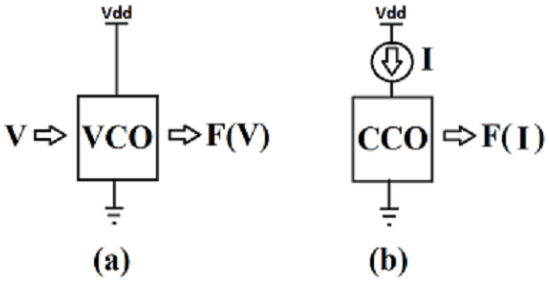

Figure 3. (a) voltage-controlled oscillator. (b) current-controlled oscillator [9]

A typical Ring VCO is plotted in Figure 4. In this design, the voltage control Vc is used to control the frequency of oscillator.

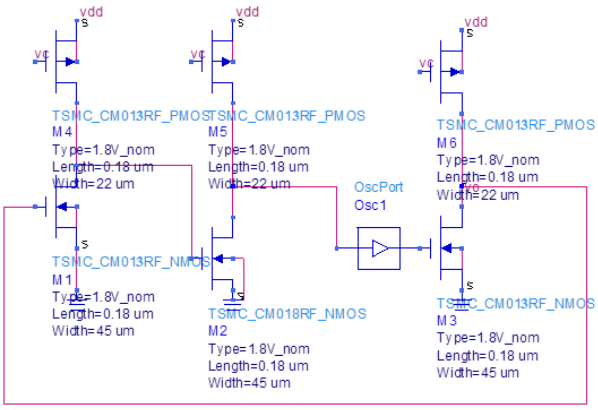

Figure 4. A typical Ring VCO

In this paper the current controlled method with body biasing technique have been used to decrease the threshold voltage Vth and improve the RVCO performance. Single-ended circuit has been simulated to present the concept, even though, the method can be extended to differential pair configuration.

This paper has been structured as follows, section 2 describes RVCO circuit design, transistor sizing and oscillation frequency. Simulation and analysis of the circuit are in section 3. Concluding remarks are at the end.

2. Proposed topology

The method used here is based on changing bulk voltage to change the current of oscillator and so the wider range og gate voltage control could be achieved.

In this paper the three stage oscillator with current control method is used. Increasing the number of stages can cause to decrease the frequency of oscillatuion and increase of power consumption. Figure 5 shows one stage of ring oscillator. In this design the body of control transistor is biased to increase the range of current variatons. The bulk voltage of the PMOS transistor should be controlled in a way that the bulk-source junction remains in reverse or slightly into forward bias. To guarantee this the bulk-source junction will not go into forward bias more than 0.5V, so the bulk current will remain negligibly low [5, 10]. An extra transistor M10 has been used to better control the bulk voltage and reduce loading effects on the control voltage as shown in Figure 5.

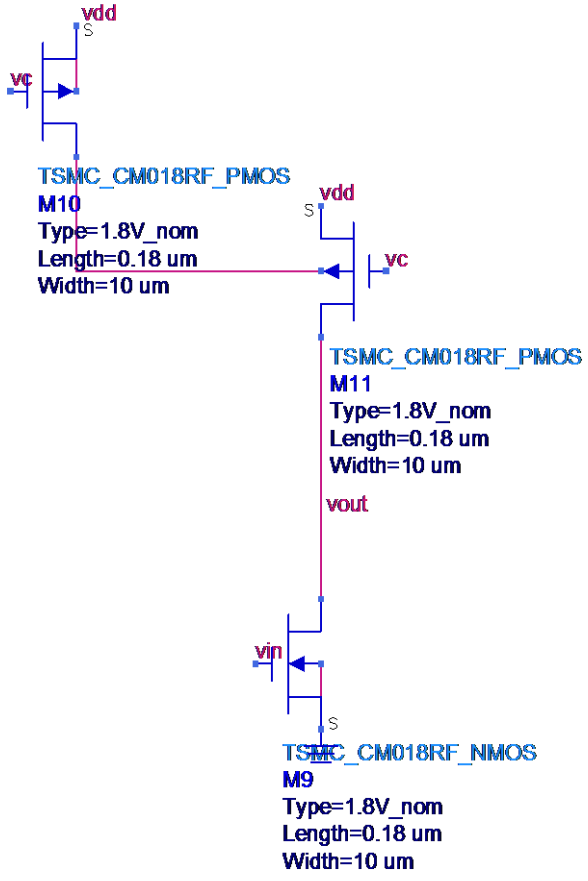

Figure 5 one stage of ring oscillator

Figure 6 shows the drain voltage versus gate voltage of one stage delay cell for Vc=0.5 V

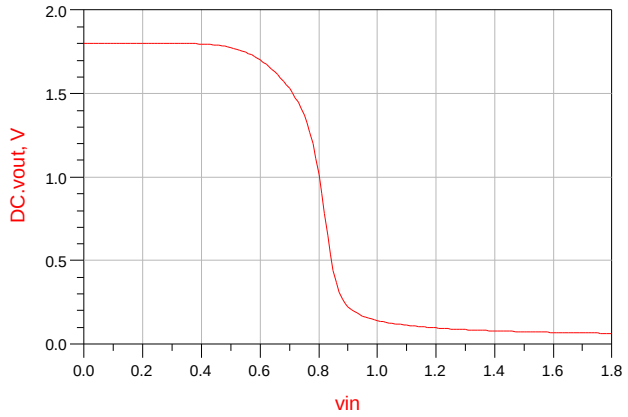

Figure 6 the drain voltage versus gate voltage

Figure 7 shows the three stage oscillator. The frequency of this oscillator is as follows:

$$f_{osc} = \frac{1}{6C_{load}V_{DSn}}\left(\frac{1}{2}K_p\left(\frac{w}{l}\right)_p\left(V_{DD} - V_{in} - \left|V_{THp}\right|\right)^2\right) \quad (1)$$

$$\left|V_{THp}\right| = \left|V_{TH0p}\right| + \gamma\left(\sqrt{2\left|\Phi_f\right| - V_{sb}} - \sqrt{2\left|\Phi_f\right|}\right) \quad (2)$$

This equation shows that the oscillation frequency is decreased by increasing the control voltage.

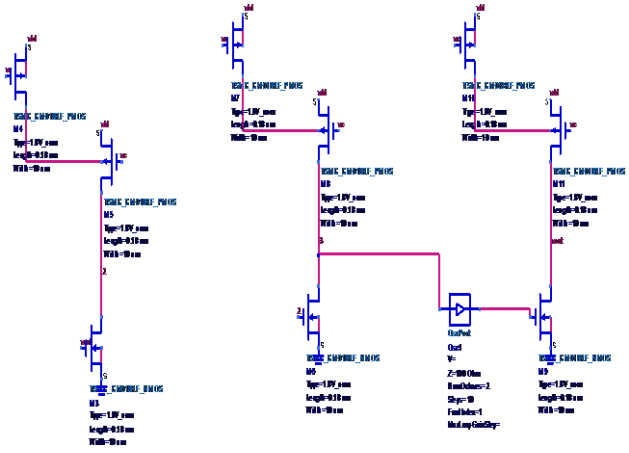

Figure 7 the three stage oscillator

The simulation results of this circuit is shown in figure 8 for Vc=0.5 V. in this state the oscillation frequency is 7.14 GHz.

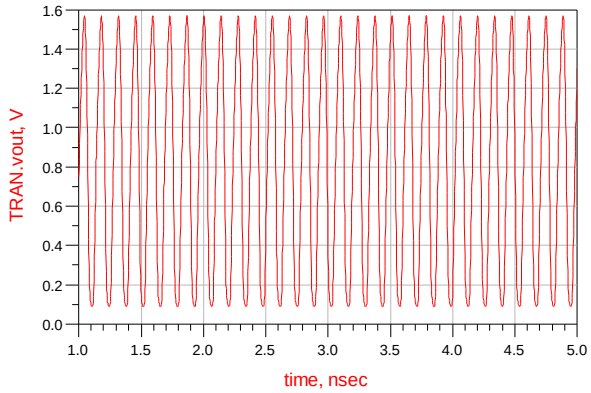

figure 8. The simulation results of VCO for Vc=0.5 V

The oscillation frequency as a function of voltage control is plotted in figure 9. As voltage control is changed from 0 to 1 v, the frequency is changed from 1.75 GHz to 11 GHz.

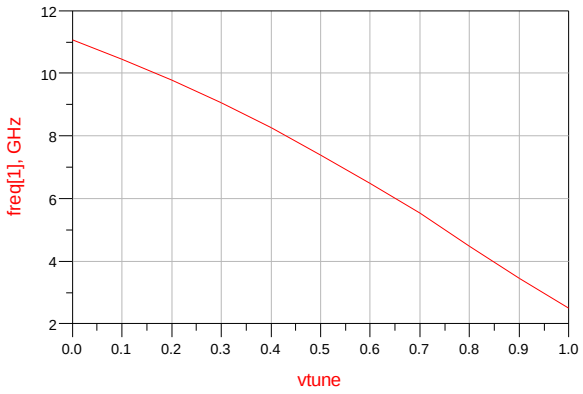

Figure 9. The oscillation frequency as a function of voltage control

The phase noise of this oscillator for Vc=0.5 V is plotted in Figure 10. One can see that the phase noise of this oscillator in this state is -82.5 dBc/Hz.

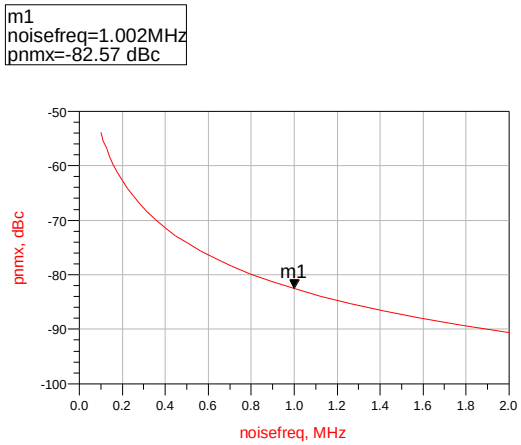

Figure 10. The phase noise of this oscillator for Vc=0.5 V

To improve the performance of proposed oscillator, an inductor is added in the bulk of control transistor. The proposed oscillator is shown in figure 11. Figure 12 shows the frequency range of proposed oscillator. One can see that the frequency range of proposed oscillator is increased by 3 GHz. The phase noise of proposed oscillator is shown in figure 13. One can see that the phase noise of proposed oscillator is improved noticeably. Table 1 shows the results of proposed oscillator.

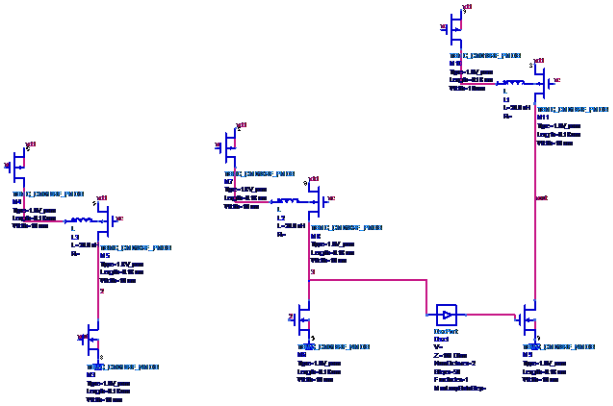

Figure 11. The proposed oscillator

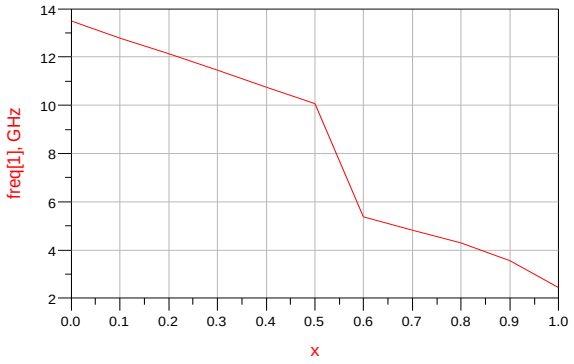

Figure 12 the frequency range of proposed oscillator

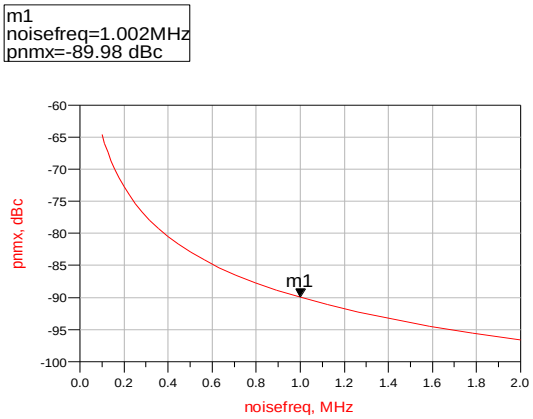

Figure 13 the phase noise of proposed oscillator

Power consumption	Frequency range	Phase noise	ref
-14 dB	1.27-4 GHz	-85 dBc/Hz	[1]
-7 dB	3.6-6.2 GHz	-78 dBc/Hz	[2]
-8.5 dB	4.7-9.3 GHz	-92 dBc/Hz	[3]
-14 dB	2-14 GHz	-90 dBc/Hz	This work

3. Conclusion

In this paper, a novel ring oscillator is proposed and simulated in 0.18 um cmos technology. To increase the frequency range of oscillator a novel technique based on forward bias of body of control transistor is proposed. Moreover, an inductor is added to the bulk of control transistor to improve its performance. It is shown that by using inductor the frequency range and phase noise is improved simultaneously. The phase noise of proposed oscillator was -90 dBc/Hz and the frequency range was 2-14 GHz.

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