IJCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Volume-4, Issue-6 E-ISSN: 2347-2693

A Novel Low Power Full Adder Using a Modified Domino Logic

Somayyeh jafarali Jassbi*, and moloud mousavi

[1,2]Department of Computer Engineering,
Islamic Azad University, Science Research Branch, Tehran, Iran
www.ijcseonline.org

Received: May/16/2016 Revised: May/30/2016 Accepted: Jun/18/2016 Published: Jun/30/ 2016

***Abstract*—** A low power and high speed Full adder circuit design using a new CMOS domino logic family is presented in this paper. The presented domino logic is based on Magnetic Tunnel Junction Elements (MTJ) in Gate Diffusion Input (GDI) Technique. Compared to static CMOS logic circuits, dynamic logic circuits are important as it provides better speed and has less transistor requirement. The proposed circuit has very low dynamic power consumption and less delay compared to the recently proposed circuit techniques for the dynamic logic styles. Moreover, it will be shown that the proposed circuit is extremely fault tolerant. The monte carlo simulation is performed to emphasis the fault tolerance of proposed full adder. The proposed full adder is simulated using standard 0.18 um CMOS technology.

***Keywords*—** *Domino, Full Adder, Buffer, Low Power*

I. INTRODUCTION

With the miniaturization of transistor dimensions, the current CMOS technology faces major issues like scalability limits, device variability and power dissipation, casting a doubt on Moore's Law [1-3]. This has prompted researchers to investigate alternative technologies as an efficient replacement of the silicon based CMOS.

Spintronic devices are one such alternative overcoming some of the above posed challenges [4]. Magnetic Tunnel Junction (MTJ), a spin based device is characterized by non-volatility, low power consumption and increased integration densities (thus resulting in high scalability), making it a promising choice in multi domain applications [5]. In recent years, researchers have shown the potential of MTJs in manyareas. Due to its non-volatility, it is used as memory devices like Magnetic Random Access Memories (MRAM) and Static Random Access Memories (SRAM) [5]. Logic devices like adders, subtractors , counters [11], flip-flops [10], ALUs [9] and basic logic circuits implementing Boolean functionalities like NAND, NOR, AND, OR have also been designed using MTJs [II] - [14]. Some of the above designs use a hybrid architecture where MTJs and CMOS are integrated with each other to produce the
desired output [10] [15]. Intermediate circuits are used to read
and write data in between these components. This circuitry adds integration complexity, power consumption, area and delay overheads. Dynamic logic requires less number of transistors to implement a given logic and is well suited for high speed circuit design. However, the major drawback of this logic is that it has excessive power dissipation due to the switching activity and clock. Some techniques are proposed for reducing excessive power dissipation of dynamic logic circuit. a mix of dynamic and static circuit styles, use of dual supply voltages and dual threshold voltage are some of these techniques [15]. In [15] new logic family called feedthrough logic (FTL) is proposed to have better speed and low power dissipation.

In this paper, we presented an optimized design for a full adder cell using MTJ and GDI technique craved for low power, low energy. The rest of the paper is organized as follows. In section II, the proposed dynamic logic and proposed full adder is presented. In section III, simulation results are presented. Section IV concludes the paper.

II. PROPOSED PREAMPLIFIER TOPOLOGY

In this section, a novel technique is proposed to reduce power consumption of domino logic. In proposed circuit, a buffer is used in domino logic circuit causing to reduce the power consumption of proposed logic compared to conventional domino logic circuits. The proposed domino logic circuit based on GDI is plotted in Fig. 1. The circuits composed of three clock transistor element so the load capacitor will be increased. In charge duration that clock is low, M6 is off and the output node would not be changed. When clock is high, M1 is off and M2 is on. In this condition, if the input A is high, M3 is on and the node Z is

grounded. On the other hand, if input A is low, the node Z would be high impedance and would not be changed. Similarly, if Z and clock is high the output F is grounded and if Z is high and clock is low the output will be high.

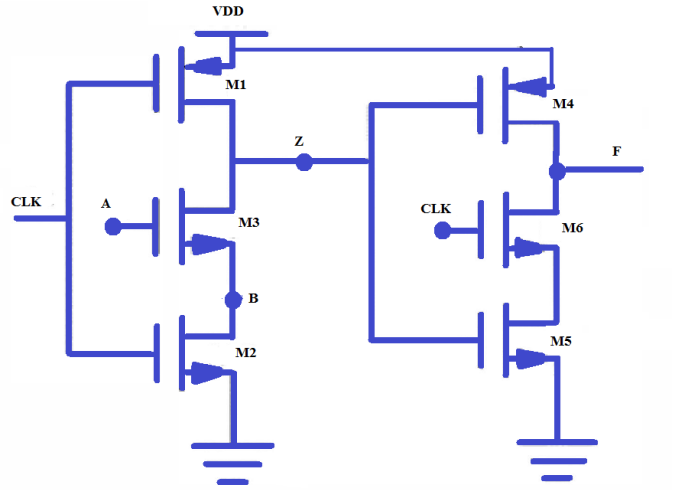

Fig. 1 The proposed domino logic circuit

For the sake of lower power consumption, the proposed domino logic circuit is modified as shown in Fig. 2. In this circuit, an MTJ element is used and in the source of M5 is connected to node B instead of ground. So, during charge period when clock is low, the node Z could not be propagated to output. In this circuit, when the input A is low the node Z is always high and the output is always low. When the input A is high, the circuit can work in two different phases.

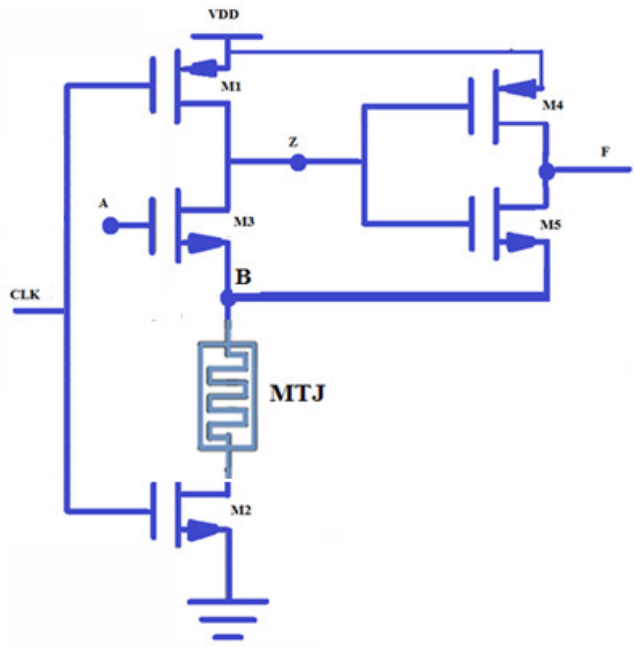

Fig. 2 the modified proposed domino logic circuit based on GDI and MTJ

Now that the novel domino logic circuit is designed, it is time to design a novel full adder using this proposed logic. The schematic of proposed full adder is shown in Fig. 3.

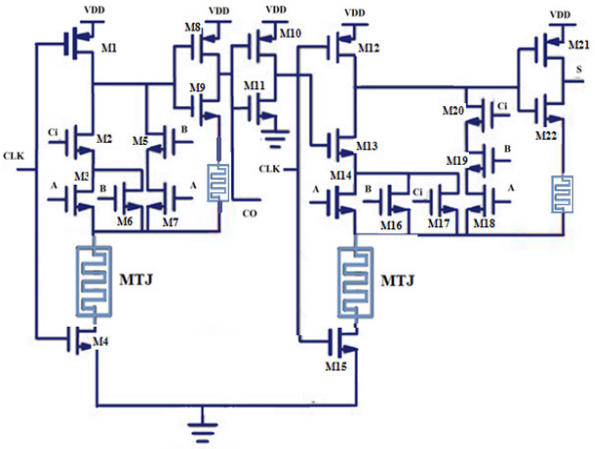

Fig. 3 schematic of proposed full adder

III. SIMULATION RESULTS

In this section, the simulation results of proposed domino logic and full adder is presented. Fig. 4 shows transient response of proposed buffer.

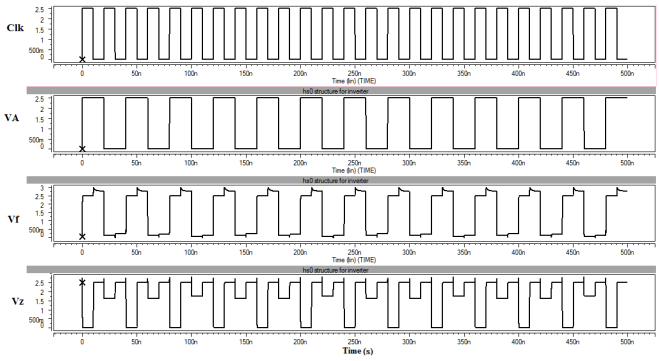

Fig. 4 transient response of proposed buffer

The delay of this buffer is plotted in Fig. 5. On can see that the delay of this circuit is 0.3 ns. Total voltage source power dissipation of this buffer is 42.2089 pW.

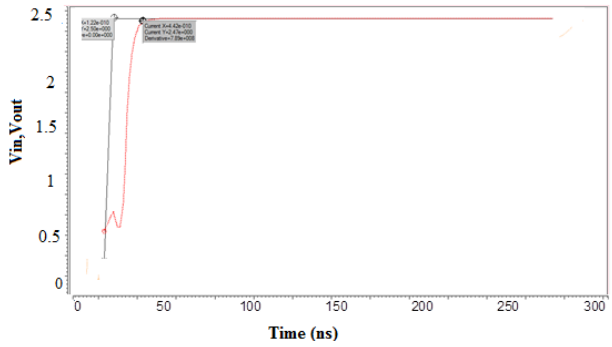

Fig. 5 The delay of proposed buffer

Fig. 6 shows the simulation results of the proposed full adder. One can see that, when all inputs are high, both outputs sum and Cout are high. When two inputs are high and other input is low, one output is low and the other is high.

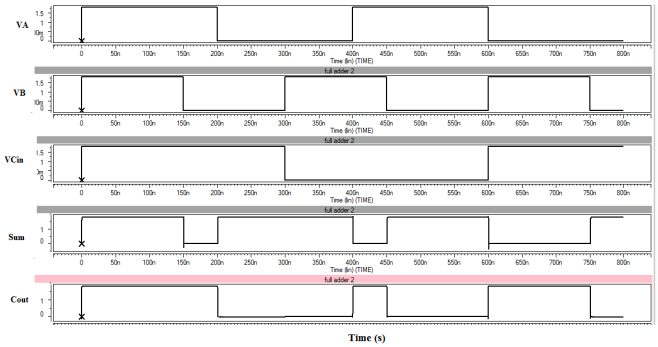

Fig. 6 simulation results of the proposed full adder.

Total voltage source power dissipation of this full adder is 447.8459 pW. The delay of this full adder is plotted in Fig. 7. As is shown in the diagram, the delay of proposed full adder is 0.35 ns.

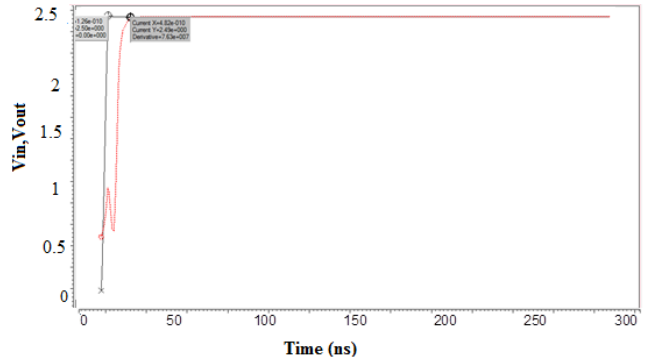

Fig. 7 delay of proposed full adder

To show that the proposed full adder is fault tolerant, different faults including process fault, voltage variations, parasitic capacitors, and noise are injected in the circuit. Fig. 8 shows the simulation result of proposed full adder under the condition that all of fault sources are injected in the circuit simultaneously. One can see that besides injecting all of these faults, the performance of full adder is not changed. The results of injecting fault in proposed full adder is summarized in Table. 1.

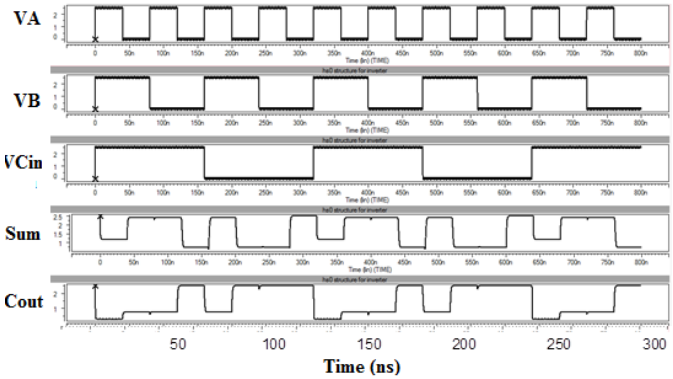

Fig. 8 simulation result of faults injected proposed full adder

Table. 1 results of injecting fault in proposed full adder

Power consumption	Delay	Fault
447 pW	0.35 ns	No fault
447 pW	0.37 ns	Process falt
44 pW	0.4 ns	Voltage variation
447 pW	0.63 ns	Parasitic capacitance
447 pW	0.33 ns	Noise injection

In Table. 2 the comparison of proposed full adder with other works is presented.

Table. 2 comparison of proposed full adder

Delay	Power consumption	
0.35 ns	0.447 uW	This work
1.009 ns	1.73 mW	[15]
0.179 ns	5.736 uW	[16]
1.117 ns	127 uW	[17]

IV. CONCLUSIONS

This work has presented a novel low power and high speed Full adder circuit design using a new CMOS domino logic family based on MTJ and GDI. The proposed circuit had very low power consumption and less delay compared to the recently proposed circuit techniques for the dynamic

logic styles. Moreover, it was shown that the proposed circuit is extremely fault tolerant. Different faults including process fault, voltage variations, parasitic capacitors, and noise were injected in the circuit. Besides injecting all of these faults, the performance of full adder was not changed. The proposed full adder consumed only 0.447 uW of power and had the delay of 0.32 ns.

REFERENCES

[I] G. E. Moore, "Cramming more components onto integrated circuits," Electronics, vol. 38, pp. 114 -117,1965.1. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp. 68-73.

[2] R. R. Schaller, "Moore's law: Past, present and future," IEEE Spectrum, vol. 34, no. 6, pp. 52-59, Jun. 1997.

[3] B. Doyle, R. Arghavani, D. Barlage, S. Datta, M. Doczy, 1. Kavalieros, A. Murthy, and R. Chau, "Transistor elements for 30 nm physical gate lengths and beyond," Intel Technol. 1., vol. 6, no. 2, pp. 42-54, May 2002.

[4] S. Sugahara and 1. Nitta, "Spin-transistor electronics: an overview and outlook," Proc. IEEE, vol. 98, pp. 2124-2154, Dec. 2010. [5] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, "Analysis of high performance fast feedthrough logic families in CMOS", IEEE Trans. Cir. & syst. II, vol. 54, no. 6, Jun. 2007, 489-493.

[5] Dhruva Kumari, Monisha SaW, Aminul Islam, "Design of 2: 1 Multiplexer and 1:2 Demultiplexer Using Magnetic Tunnel Junction Elements," IEEE, 2013.

[6] M. Hosoml, H. Yamaglshl, T. Yamamoto, K. Bessho, Y. HlgO, K. Yamane, H. Yamada, M. Shoji, H. Hachino, C. Fukumoto, H. Nagao, and H. Kano, "A novel nonvolatile memory with spin torque transfer magnetization switching: spin-ram," IEEE International Electron Devices Meeting, IEDM Technical Digest, pp. 459-462, Dec. 2005.

[7] W. Zhao, E. Belhaire, C. Chappert, and P. Mazoyer, "Spintronic device based non-volatile low standby power sram," IEEE Computer Society Annual Symposium on VLSI, pp. 40-45, April 2008.

[8] H. Meng, 1. Wang, and 1. P. Wang, "A spintronics full adder for magnetic CPU," IEEE Electron. Devices Lett., vol. 26, no. 6, pp. 360-362, Jun. 2005.

[9] S. Patil, X. Yao, H. Meng, 1.-P. Wang, and D. Lilja,"Design of a spintronic arithmetic and logic unit using magnetic tunnel junctions," Proceedings ofthe 5th conference on Computing frontiers, pp. 171-178, 2008.

[10] W. Zhao, E. Belhaire, V. Javerliac, C. Chappert, and B. Dieny, "A non-volatile flip-flop in magnetic fpga chip," International Conference on Design and Test of Integrated Systems in Nanoscale Technology (DTTS), pp. 323-326,2006.

[11] S. Lee, N. Kim, H. Yang, G. Lee, S. Lee, and H. Shin, "The 3- bit gray counter based on magnetic-tunnel-junction elements," IEEE Transactions on Magnetics, vol. 43, no. 6, pp. 2677-2679, June 2007.

[12] S. Patil, A. Lyle, J. Harms, D. Lilja and 1.-P. Wang, "Spintronic logic gates for spintronic data using magnetic tunnel junctions," in Proc. IEEE Int. Conf. Computer Design, 2010, pp. 125-131, Oct. 2010.

[13] 1. Wang, H. Meng, and 1. P. Wang, "Programmable spintronics logic device based on a magnetic tunnel junction element," J. Appl. Phys., vol. 97, no. 10, p. 10D 509, May 2005.

[14] A. Ney, C. Pampuch, R. Koch, and K. H. Ploog, "Programmable computing with a single magnetoresistive element," Nature, vol. 425, pp. 485-487, Oct. 2003.

[15] N. Srinivasa Gupta, M. Satyanarayana, "A Novel Domino Logic for Arithmetic Circuits" International Journal of Innovative Technology and Exploring Engineering, Volume-3, Issue-3, August 2013.

[16] C.-K. Tung, S.-H. Shieh and C.-H. Cheng, "Low-power high-speed full adder for portable electronic applications" ELECTRONICS LETTERS, Vol. 49, No. 17, 2013.

[17] Yi WEI, Ji-zhong SHEN, "Design of a novel low power 8-transistor 1-bit full adder cell" Journal of Zhejiang University-SCIENCE , 2011.

