JCSE International Journal of Computer Sciences and Engineering Open Access
Research Paper Volume-2, Issue-12 E-ISSN: 2347-2693

High Gain, Wide Bandwidth and Optimal Swing op-amp in CMOS Technology

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www.ijcaonline.org

Received: Nov/26 /2014 Revised: Dec/04/2014 Accepted: Dec/18/2014 Published: Dec/31/ 2014

Abstract— Nowadays, operational amplifiers (op-amps) are widely used in numerous advanced electronic systems. Most of op-amps need a high gain, wide bandwidth, and an optimal swing. However, meeting these requirements all at the same time has been a challenging problem for analogue circuits designers. For different systems, many various structures have been used, and each has improved one of features of the amplifier in some way. In the present study, attempted was made to reach the best conditions for gain, bandwidth, and swing through appropriate parametric models. Of course, it is considered that the rest of circuit conditions do not undergo undesirable changes and get the best values [1].

Keywords- CMOS Technology, op-amp, CMFB Circuit

I. Introduction

Amplifiers with more than one stage are those that provide the designer with high swing and high gain; however, one of the most important problems of such amplifiers is their low speed and lack of stability required for the circuit. The method used for parameterization is based on a two-stage, high-gain, optimal-swing, and wide-bandwidth amplifier design. Such a method is different from former ones in type of parameterization, voltage selection, and reliance on obtaining measures of integer values. In this paper, three new approaches to the integrated circuit operational amplifier designs have been discussed under conditions of high gain, wide bandwidth, and optimal swing in the CMOS. These conditions, of course, can only be realized when the parameters' values could be changed in COMS devices, and it is achieved when the devices are properly biased in design modes.

For the first approach, form of the computations are given in terms of equations relevant to this method. By using such relations, specifications of the input stage transistors (including PMOS transistors that have a common architecture) were accurately calculated. However, for the second approach, a new architecture is also proposed in the stages design by which 0.18 micrometer data has been calculated in CMOS technology under conditions of desirable feed and the most appropriate threshold voltages. The third approach is also obtained homogenously and in compliance with an appropriate parameterization. Amplifying structure designed in the is of two-stage amplifiers, and the compensation method was used to solve problems of instability and low speed. Such compensation is of a hybrid type and was adopted from [2]. Circuit performance in the stimulation results is confirmed by HSPICE software.

From the perspective of analogue systems, an op-amp amplifier should have the following structural conditions:

1. The input resistance should be infinite,
2. The output resistance should be zero,
3. Open-loop voltage gain should be infinite,
4. Bandwidth should be infinite,
5. While voltage difference in the input is zero, the output voltage should also be zero, and,
6. Characteristic curve should not change with temperature.

These are desirable conditions that the design should try to enhance.

II. Analysis

In the present research, gain, bandwidth, and swing were specifically studied; meanwhile, some other parameters were also considered. For example, it has been attempted to have the least power consumption. To have a high gain, wide bandwidth, and an optimal swing op-amp, using a two-stage voltage amplifier is one the best existing structures. Cascode method was also used to enhance the gain and POMS input was prioritized. For the second stage, in compliance with the above-mentioned design which is the basis of the parameterization in this paper, a common source amplifier was used [2, 3]. Given the previous works in this field and review of the existing references, the best structural model is shown in Fig 1.

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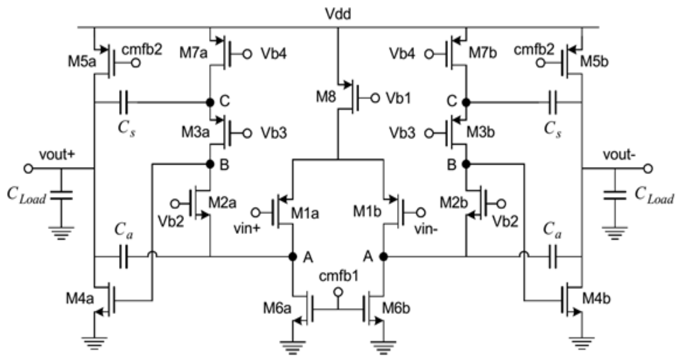

Fig 1. Structure of an op-amp in CMOS technology with a high gain and wide bandwidth.

To analyze ac, small signal equivalent circuit could be used as shown in Fig 2.

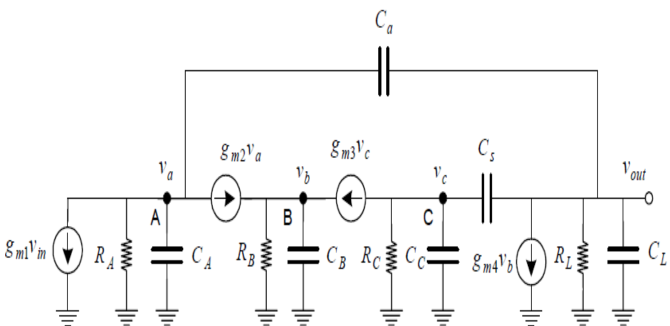

Fig 2. Small signal model.For the amplifier shown in Fig 2, the gain is given through the following relation:

(1)

$$Gain = g_{m1}\left(g_{m3} + \frac{1}{R_C}\right) \times \frac{g_{m2}g_{m4}}{d_0}$$

The parameters in 1 are as follows:

(2)

$$R_C = r_{ds7} \parallel \frac{g_{m2}r_{ds2}(r_{ds1} \parallel r_{ds6})}{1 + g_{m3}r_{ds3}}$$

(3)

$$d_0 = \frac{g_{m2}g_{m3}}{R_L R_B}$$

(4)

$$R_B = g_{m2}r_{ds2}(r_{ds1} \parallel r_{ds6}) \parallel \; g_{m3}r_{ds3}r_{ds7}$$

(5)

$$R_L = (r_{ds4} \parallel r_{ds5})$$

By adjusting the above parameters, we improved gain value for the amplifier. In designing the amplifying circuit, frequency response should also be considered; therefore, by conducting relevant analyses, the amount and location of the pole and circuit zeros can be calculated via:

(6)

$$S_{p1} = -\frac{1}{g_{m4}C_m R_L R_B}$$

(7)

$$S_{p2} \cong -\frac{4g_{m2}g_{m3}}{C_m(g_{m2}+g_{m3})}$$

(8)

$$|S_{p3,4}| = \sqrt{\frac{g_{m4}(g_{m2}+g_{m3})}{C_B C_L}}$$

(9)

$$S_{z1} = -\frac{2g_{m3}}{C_m}$$

(10)

$$S_{z2,3} \approx \pm\sqrt{\frac{2g_{m2}g_{m4}}{C_m C_B}}$$

In the above relations, values of C_m and C_B are:

(11)

$$C_m = 2C_a = 2C_s$$

(12)

$$C_B = C_{db2} + C_{db3} + C_{gs4} + C_{gd2} + C_{gd3}$$

By choosing appropriate values for circuit zeros and poles, the amount of bandwidth and settling time in the circuit could be determined. To reduce the order of voltage amplifying circuit, by equalizing the first zero and the second pole, one order of the system may be reduced and changed into a third order system [4, 5].

By using the above relations, voltage amplifier could be designed, and the intended parameters may be specified. Given that a pole and a zero should neutralize each other, this relation is obtained via $g_{m2} = g_{m3}$. By observing such facts and choosing values in Table 1 for circuit transistors, we have values for circuit transistors.

Table 1. gm parameter for circuit transistors.

	gm		gm
M1aو M1b	5.6	M4aو M4b	25
M2a وM2b	0.54	M5aو M5b	21
M3aو M3b	0.64	M6aو M6b	6.1
M7aو M7b	0.62	M8	7.7

To design circuit transistors, relevant formulas could be used; however, by using Gm-Ic design method, values mentioned above could be easily designed with high accuracy.

Table 2. sizes for transistors.

	W(μm)	L(nm)		W(μm)	L(nm)
M1a و M1b	40	180, m=2	M4a و M4b	60	180
M2a و M2b	5	180	M5a و M5b	60	180, m=2
M3a و M3b	30	180	M6a و M6b	50	360
M7a و M7b	70	360	M8	90	180
VB1=1.1 VB2=1.22 VB3=1 VB4=1.3					

It is important to consider transistors' settings at the saturation zone. In addition, because of the priority of parameterization mechanism in this paper, operating points for all transistors are given:

```
subckt   x1             x1             x1             x1
element      1:m1a          1:m1b          1:m2a          1:m2b
model       0:pch.4        0:pch.4        0:nch.8        0:nch.8
region    Saturation     Saturation     Saturation     Saturation
 id      -4.825752593e-04 -4.825752593e-04  3.576548951e-05  3.576548951e-05
 ibs      5.005269911e-20  5.005269911e-20 -4.887026304e-21 -4.887026305e-21
 ibd      1.977675101e-16  1.977675101e-16 -1.289494600e-17 -1.289494600e-17
 vgs     -6.206872742e-01 -6.206872742e-01  5.485715938e-01  5.485715938e-01
 vds     -8.492588680e-01 -8.492588680e-01  1.253371009e-01  1.253371010e-01
 vbs       0.             0.             0.             0.
 vth     -5.061574777e-01 -5.061574777e-01  5.184319979e-01  5.184319979e-01
 vdsat   -1.316178287e-01 -1.316178287e-01  7.585033532e-02  7.585033531e-02
 vod     -1.145297965e-01 -1.145297965e-01  3.013959595e-02  3.013959594e-02
 beta     4.476408730e-02  4.476408730e-02  1.608563650e-02  1.608563650e-02
 gam eff  6.761707306e-01  6.761707306e-01  9.667809240e-01  9.667809240e-01
 gm       5.640295191e-03  5.640295191e-03  5.419323881e-04  5.419323881e-04
 gds      1.097008850e-04  1.097008850e-04  6.345544486e-05  6.345544480e-05
 gmb      1.878677258e-03  1.878677258e-03  1.587730862e-04  1.587730862e-04
 cdtot    8.298385626e-14  8.298385626e-14  5.753190737e-15  5.753190737e-15
 cgtot    1.315513144e-13  1.315513144e-13  7.673087529e-15  7.673087529e-15
 cstot    1.835163766e-13  1.835163766e-13  9.472943571e-15  9.472943571e-15
 cbtot    1.596907257e-13  1.596907257e-13  9.888331504e-15  9.888331504e-15
 cgs      9.797284182e-14  9.797284182e-14  4.738829563e-15  4.738829563e-15
 cgd      2.598244435e-14  2.598244435e-14  1.846126900e-15  1.846126900e-15
```

```
subckt   x1             x1             x1             x1
element      1:m3a          1:m3b          1:m6a          1:m6b
model       0:pch.4        0:pch.4        0:nch.4        0:nch.4
region    Saturation     Saturation     Saturation     Saturation
 id      -3.576548833e-05 -3.576548833e-05  5.183407511e-04  5.183407511e-04
 ibs      3.735023691e-21  3.735023692e-21 -6.887613840e-20 -6.887613840e-20
 ibd      5.654445644e-17  5.654445644e-17 -7.930369770e-14 -7.930369772e-14
 vgs     -5.139482974e-01 -5.139482974e-01  5.967655072e-01  5.967655072e-01
 vds     -7.171827902e-01 -7.171827902e-01  6.714284062e-01  6.714284062e-01
 vbs       0.             0.             0.             0.
 vth     -5.067495087e-01 -5.067495087e-01  4.914706578e-01  4.914706578e-01
 vdsat   -7.434601071e-02 -7.434601072e-02  1.267542813e-01  1.267542813e-01
 vod     -7.198788667e-03 -7.198788668e-03  1.052948494e-01  1.052948494e-01
 beta     1.692370096e-02  1.692370096e-02  6.413577115e-02  6.413577115e-02
 gam eff  6.761706737e-01  6.761706737e-01  5.884063276e-01  5.884063276e-01
 gm       6.469830135e-04  6.469830135e-04  6.179866280e-03  6.179866280e-03
 gds      1.167943674e-05  1.167943674e-05  6.988424102e-05  6.988424102e-05
 gmb      2.168025579e-04  2.168025579e-04  1.719205166e-03  1.719205166e-03
 cdtot    3.185882712e-14  3.185882712e-14  6.635733185e-14  6.635733185e-14
 cgtot    3.991703455e-14  3.991703455e-14  1.353982059e-13  1.353982059e-13
 cstot    5.476295098e-14  5.476295098e-14  1.837567281e-13  1.837567281e-13
 cbtot    6.045047860e-14  6.045047860e-14  1.438558747e-13  1.438558747e-13
 cgs      2.404878005e-14  2.404878005e-14  1.062479017e-13  1.062479017e-13
 cgd      9.765894719e-15  9.765894719e-15  1.828218637e-14  1.828218637e-14
```

```
subckt   x1             x1             x1             x1
element      1:m7a          1:m7b          1:m8           1:m4a
model       0:pch.4        0:pch.4        0:pch.4        0:nch.4
region    Saturation     Saturation     Saturation     Saturation
 id      -3.576548919e-05 -3.576548919e-05 -9.651505249e-04  5.305780927e-03
 ibs      4.032453919e-21  4.032453920e-21  9.897147131e-20 -6.308074397e-19
 ibd      1.418426012e-16  1.418426012e-16  1.671015263e-16 -1.254304924e-15
 vgs     -5.000000000e-01 -5.000000000e-01 -7.000000000e-01  7.967655071e-01
 vds     -2.860517026e-01 -2.860517026e-01 -2.793127258e-01  5.971519008e-01
 vbs       0.             0.             0.             0.
 vth     -4.729440714e-01 -4.729440714e-01 -5.087250411e-01  5.137976287e-01
 vdsat   -8.235317034e-02 -8.235317034e-02 -1.804268345e-01  1.798502022e-01
 vod     -2.705592863e-02 -2.705592863e-02 -1.912749589e-01  2.829678784e-01
 beta     1.531607962e-02  1.531607962e-02  4.990643855e-02  1.872822531e-01
 gam eff  5.516458303e-01  5.516458303e-01  6.761707857e-01  9.619787714e-01
 gm       6.249069332e-04  6.249069332e-04  7.728926666e-03  2.502152222e-02
 gds      9.276069250e-06  9.276069250e-06  7.423944109e-04  1.237620646e-03
 gmb      2.071892586e-04  2.071892586e-04  2.629525505e-03  7.086616624e-03
 cdtot    1.127178071e-13  1.127178071e-13  1.055826556e-13  5.912048676e-14
 cgtot    1.566678300e-13  1.566678300e-13  1.528870026e-13  1.073960571e-13
 cstot    2.281510159e-13  2.281510159e-13  2.122190331e-13  1.339792021e-13
 cbtot    2.388985614e-13  2.388985614e-13  1.903104267e-13  1.070083470e-13
 cgs      1.113386113e-13  1.113386113e-13  1.168589879e-13  7.725505868e-14
 cgd      2.293603324e-14  2.293603324e-14  2.961526028e-14  2.190133081e-14
```

```
subckt   x1             x1             x1
element      1:m4b          1:m5a          1:m5b
model       0:nch.4        0:pch.4        0:pch.4
region    Saturation     Saturation     Saturation
 id       5.305780928e-03 -5.305780923e-03 -5.305780924e-03
 ibs     -6.308074398e-19  5.460374263e-19  5.460374264e-19
 ibd     -1.254304849e-15  4.025366385e-13  4.025366498e-13
 vgs      7.967655072e-01 -9.028480997e-01 -9.028480997e-01
 vds      5.971518998e-01 -1.202848099e+00 -1.202848100e+00
 vbs       0.             0.             0.
 vth      5.137976287e-01 -5.045848487e-01 -5.045848487e-01
 vdsat    1.798502022e-01 -3.035237325e-01 -3.035237325e-01
 vod      2.829678785e-01 -3.982632510e-01 -3.982632510e-01
 beta     1.872822531e-01  6.472552145e-02  6.472552145e-02
 gam eff  9.619787714e-01  6.761711794e-01  6.761711794e-01
 gm       2.502152221e-02  2.135860801e-02  2.135860801e-02
 gds      1.237620649e-03  6.751042678e-04  6.751042672e-04
 gmb      7.086616624e-03  7.134652051e-03  7.134652052e-03
 cdtot    5.912048677e-14  1.181214243e-13  1.181214242e-13
 cgtot    1.073960571e-13  2.080910088e-13  2.080910088e-13
 cstot    1.339792021e-13  2.876608337e-13  2.876608337e-13
 cbtot    1.070083470e-13  2.316695756e-13  2.316695756e-13
 cgs      7.725505868e-14  1.616793986e-13  1.616793986e-13
 cgd      2.190133081e-14  3.896257666e-14  3.896257666e-14
```

To analyze the theory, first we assigned a power value to stage FOLDED CASCODE, (for example, 10 MW). Now, it could be said that the whole DC current can flow through transistors M6a and M6b. As a result, power consumption could be calculated via:

(13)

$$\mathbf{p = VDD \times (I_{M6a} + I_{M6b})}$$

Transistors M6a and M6b are similar, thus their currents are equal. Therefore, the current for each is almost 2.8 MA, and we considered 1.4 MA as the current for the rest of the transistors. Now, differential output swing 2V should be taken into account, which results in relation 14:

(14)

$$max\,swing = 2\begin{bmatrix} VDD - (VOD_{M6a} + VOD_{M2a} \\ + |VOD_{M3a}| + |VOD_{M7a}|) \end{bmatrix}$$

$$VOD_{M6a} + VOD_{M2a} + |VOD_{M3a}| + |VOD_{M7a}| = 0.8v$$

We consider the effective voltages for POMS transistors 0.25 V, because their mobility is low; also, transistor M6a has a higher effective voltage, since under such conditions its current is larger than 0.18 V. As a result, the effective voltage for transistor M2a will be 0.12 V. for the ratio of length to width of transistors PMOS and NMOS, we have:

(15)

$$\left(\frac{W}{L}\right)_n = \frac{2I_D}{\mu_n C_{ox}(V_{GS} - V_{th})^2}$$

(16)

$$\left(\frac{W}{L}\right)_p = \frac{2I_D}{\mu_p C_{ox}(V_{GS} - V_{th})^2}$$

Consider

$\mu_n C_{ox} = 150\,{}^{\mu A}/_{V^2}$ and $\mu_p C_{ox} = 50\,{}^{\mu A}/_{V^2}$, then:

(17)

$$\left(\frac{W}{L}\right)_{M6a} = 1152$$

(18)

$$\left(\frac{W}{L}\right)_{M2a} = 1296$$

(19)

$$\left(\frac{W}{L}\right)_{M1a} = 1296$$

(20)

$$\left(\frac{W}{L}\right)_{M3a} = 896$$

(21)

$$\left(\frac{W}{L}\right)_{M7a} = 896$$

The design is based on the obtained values and attempt was made to have round non-decimal numbers so that better results would be yielded. However, it should be noted that channel length modulation was not taken into account and SPICE provided a more accurate model for stimulation. By using SPICE and changing the length and width, the output optimal values are given. Variables and parameters measured are all based on the existing mathematical models and inspired by the best references in the field of analogue studies.

Application of CMFB circuit

For this entirely differential structure, two CMFB circuits were used to increase circuit speed [6, 7]. Such circuits apply output sample and adjust voltages shown in Fig 1 to obtain the best matching. Circuit model for the ideal CMFB is shown in Fig 3.

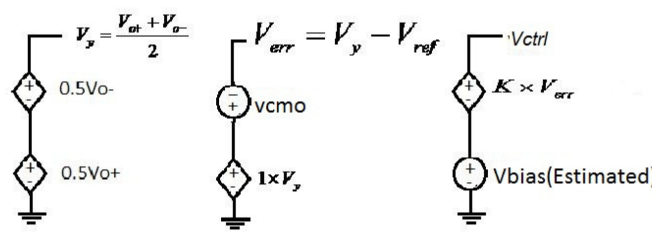

Fig 3. Circuit CMFB.

III. STIMULATION RESULTS FOR THE OPERATIONAL AMPLIFIER (OP-AMP) UNDER DESIRABLE CONDITIONS

To stimulate the circuit (see Fig. 1), HSPICE software and 0.18 Micrometer library of CMOS were used. Stimulation results for ac voltage amplifier are shown in Fig 4. To obtain the gain, we considered the input 1 V by using the software method; as a result, the output became equal to op-amp gain. Value of gain in this amplifier is 72 DB. When the gain is to be 0 Db, bandwidth is given in MHz. Thus, bandwidth for the designed amplifier is 526 MHz. Phase margin is 75°. Given that the result of the gain multiplied by the bandwidth is a constant, the increased gain results in bandwidth reduction. Therefore, it is important to select parameters properly to have all desirable conditions [8, 9].

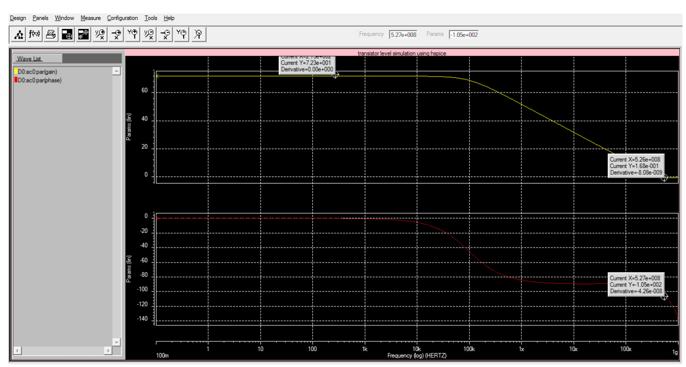

Fig 4. Stimulation results for ac operational amplifier.

SR calculation

To calculate SR, we the differential amplifier of two-step voltages (with the highest changes in input) with a range from about 20 to 50 MV in the amplifier inputs so that the largest changes are given in the differential output. To obtain negative SR, we apply the input voltages inversely. Fig 5. and Fig 6. show values obtained for positive and negative SR:

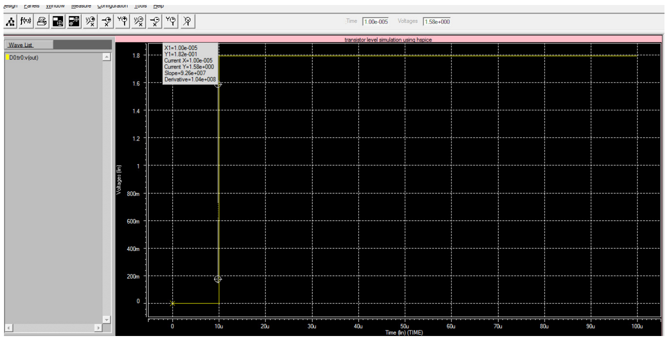

Fig 5. Positive SR values.

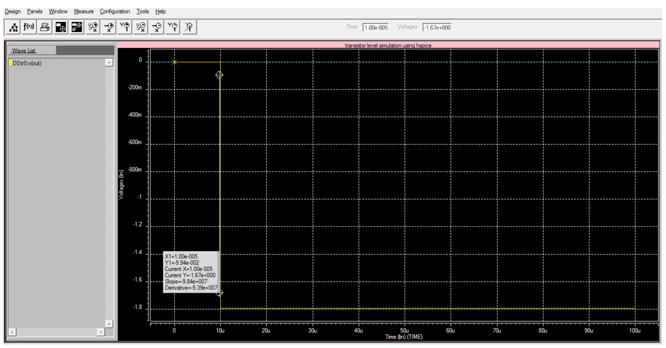

Fig 6. Negative SR value.

To have an appropriate amount of output voltage swing, the two-stage structure should be used. Swing value for the circuit output is shown in Fig 7. To obtain the value of the swing, first we should put the op-amp in the open-loop state, and very low amplitude and frequency should be applied to the input. The initial value in which the output is distorted indicates maximum swing in the output. In other words, we apply sinusoidal signal in the input and we will have it amplified in the output. We increase input amplitude to the extent that the signal starts to cut off in the output [9]. For the amplifier, power consumption is 20 MW.

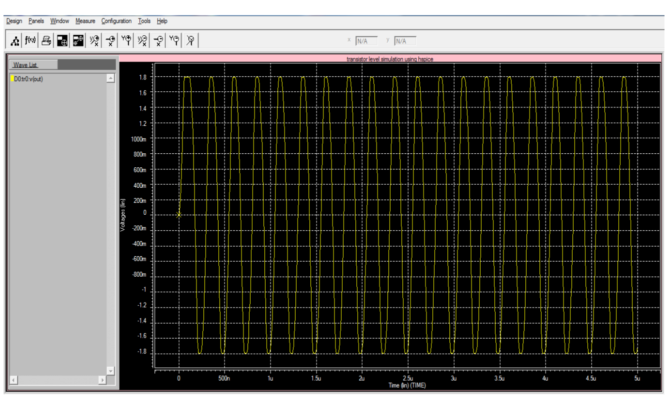

Fig 7. Swing value for circuit output of op-amp in the differential state.

IV. RESULT

Engineers expect to reach the optimal results at the qualitative level of a circuit with respect to different parameters. Gain, bandwidth, and swing are three principles for designing such circuits, which can ultimately yield optimal results. By taking some steps in this regard, practical desirable results are certainly obtained .In this paper, we parametrically improved an op-amp that has been designed by using structures of two-stage amplifiers and relying on compensation methods of circuits. For the two-stage operational amplifier with differential model based on the CASCODE design, we adjusted the parameters to reach an appropriate gain, a desirable swing, and a wide bandwidth, which are the most important specifications of operational amplifiers. In addition, in the process, attempt was made to considerably reduce power consumption.

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